High Resolution Electronic Measurements in Nano-Bio Science

Instrumentation-on-chip

The power of Silicon

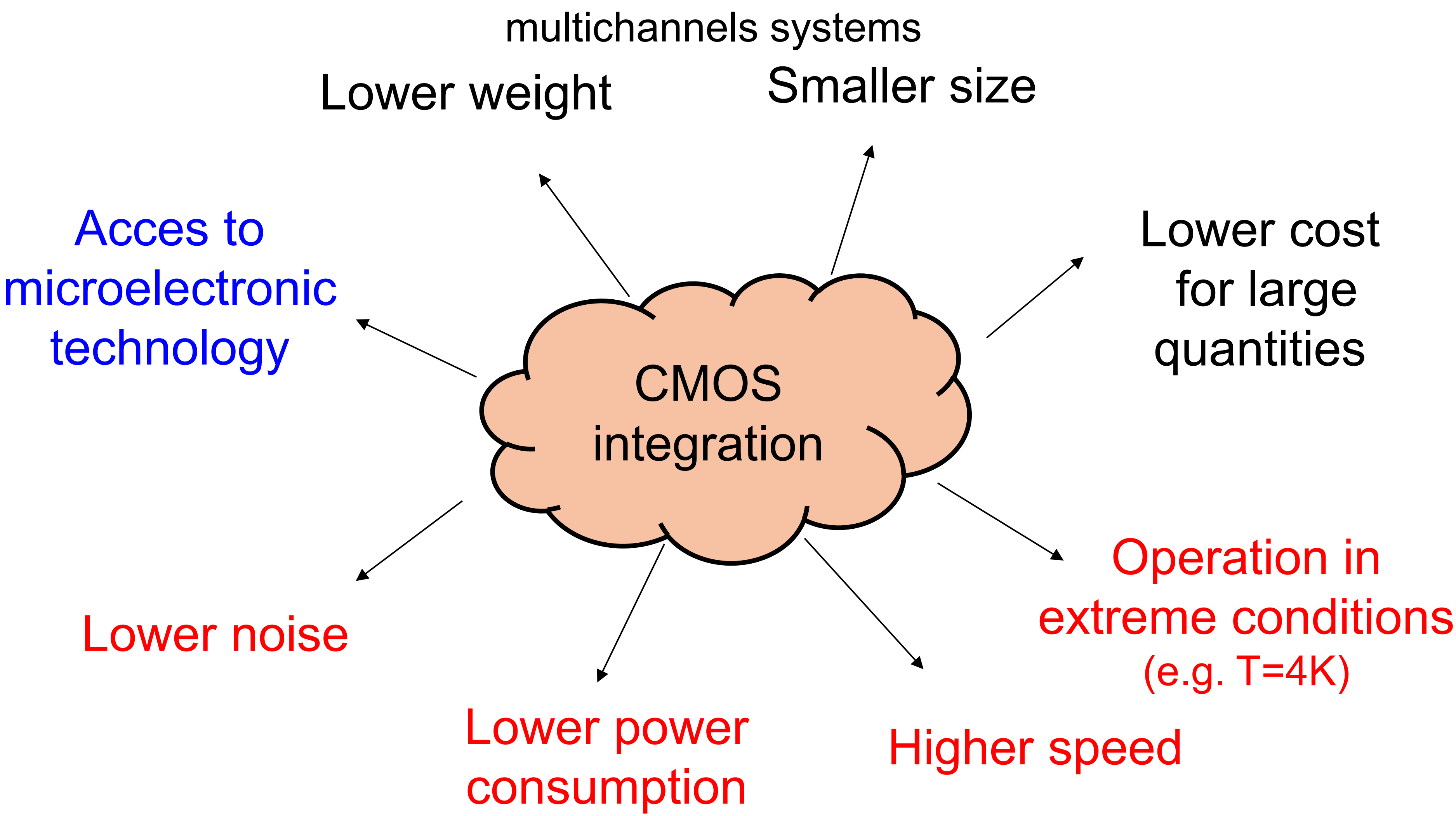
Giorgio Ferrari

Milano, June 2025

OUTLOOK of the LESSON

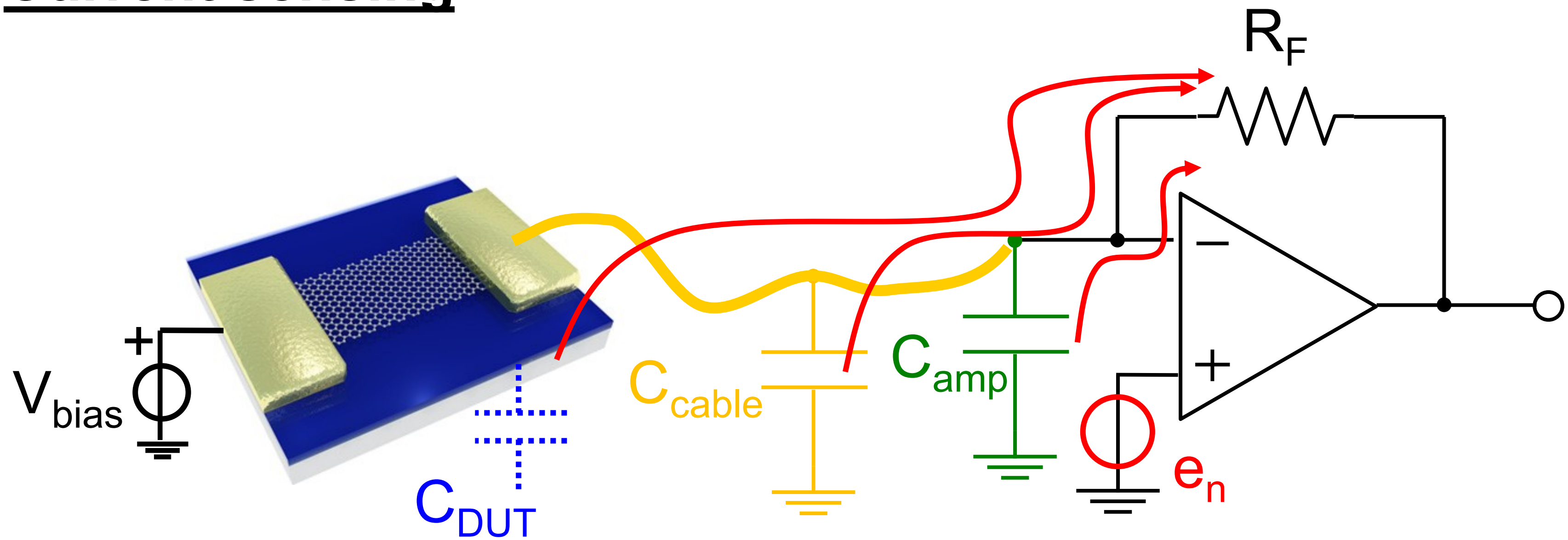
- Low-level current measurements using CMOS amplifiers
- On-chip LIAs
- Examples of sensor-electronics codesign

Application Specific Integrated Circuit (ASIC)

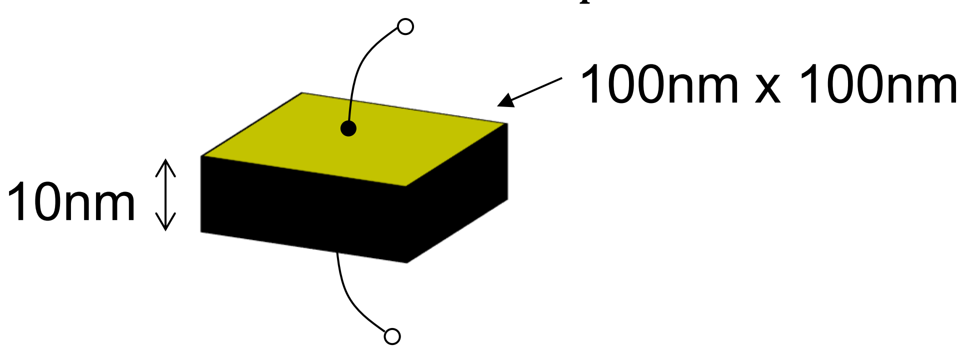


Many advantages are *possible* by <u>tailoring</u> the microelectronic chip for a specific application!

Current sensing



$$\overline{i_{eq}^2} \approx \frac{4kT}{R_F} + \overline{e_n^2}\,\omega^2\left(C_{DUT} + C_{cable} + C_{amp}\right)^2$$



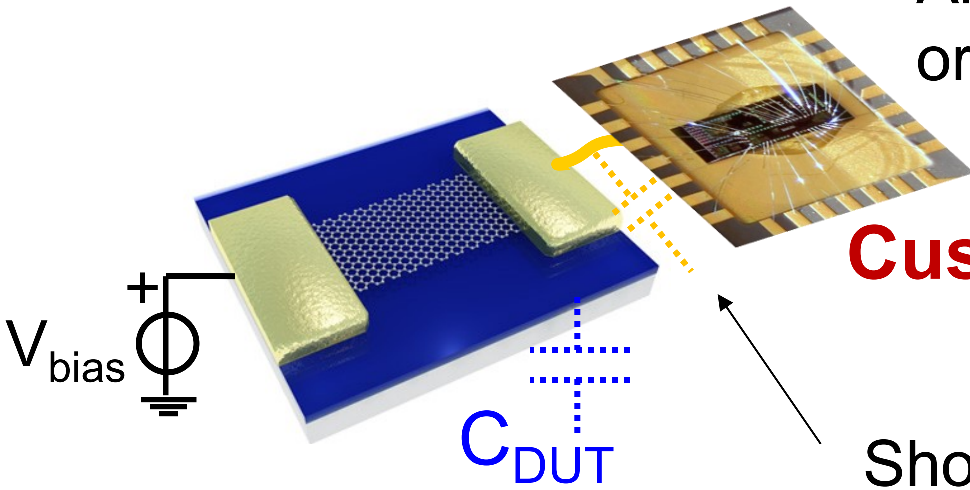
$C_{DUT} \ll 1$ pF

$C_{cable} \approx 80$ pF/m

$C_{amp} \approx 10$pF discrete comp. amp.

Improving the Signal-to-Noise ratio

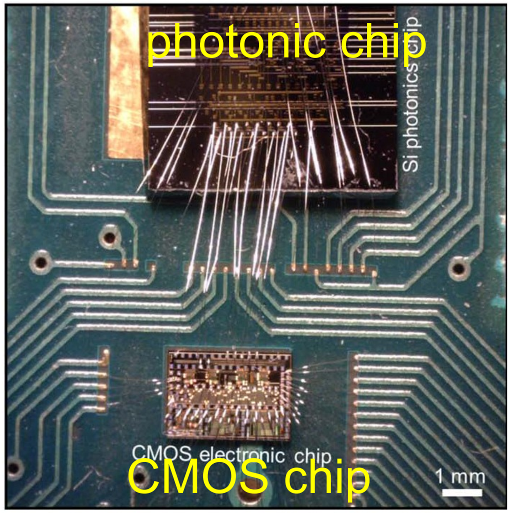
Current sensing



Amplified signal or Digital output

Custom CMOS circuit

Short connection, ideally without connector



$$\overline{i_{eq}^2} \approx \frac{4kT}{R_F} + \overline{e_n^2}\,\omega^2\left(C_{DUT} + C_{cable} + C_{amp}\right)^2$$

<1pF

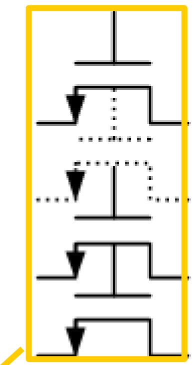
DC-1MHz Current Amplifier

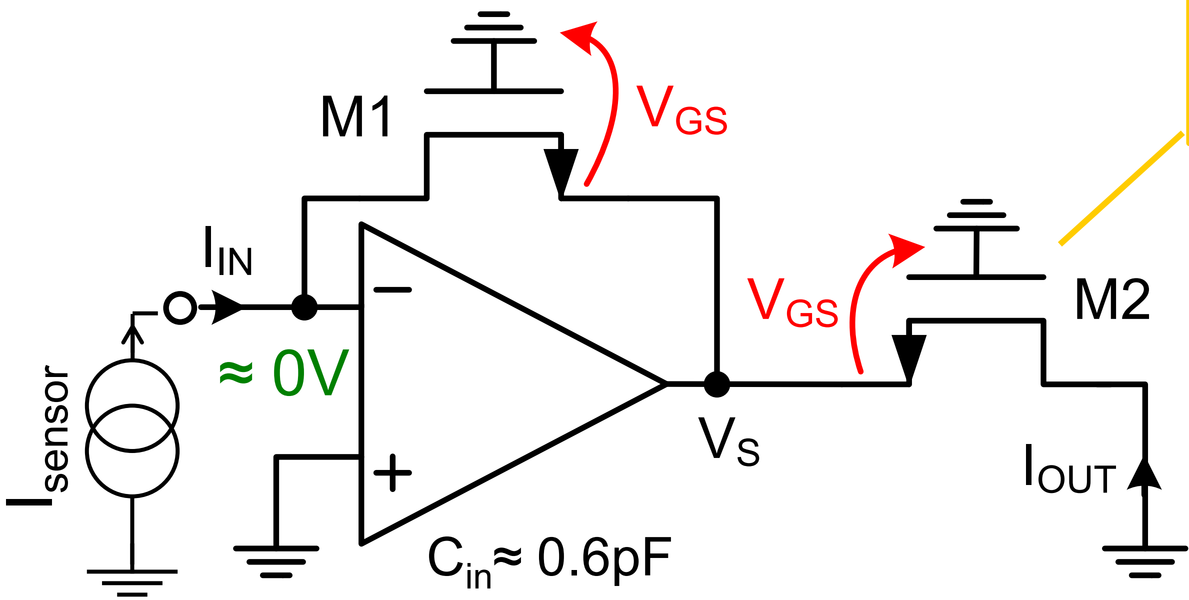
Integrated resistors value < ≈1MΩ ! (BW≈ 10kHz, noise ≈ 13pA),

do not use them!

→ **subthreshold** MOS transistors (>TΩ)

- Pseudoresitors *(E. Guglielmi, IEEE JSSC, 2020)*
- matched transistors





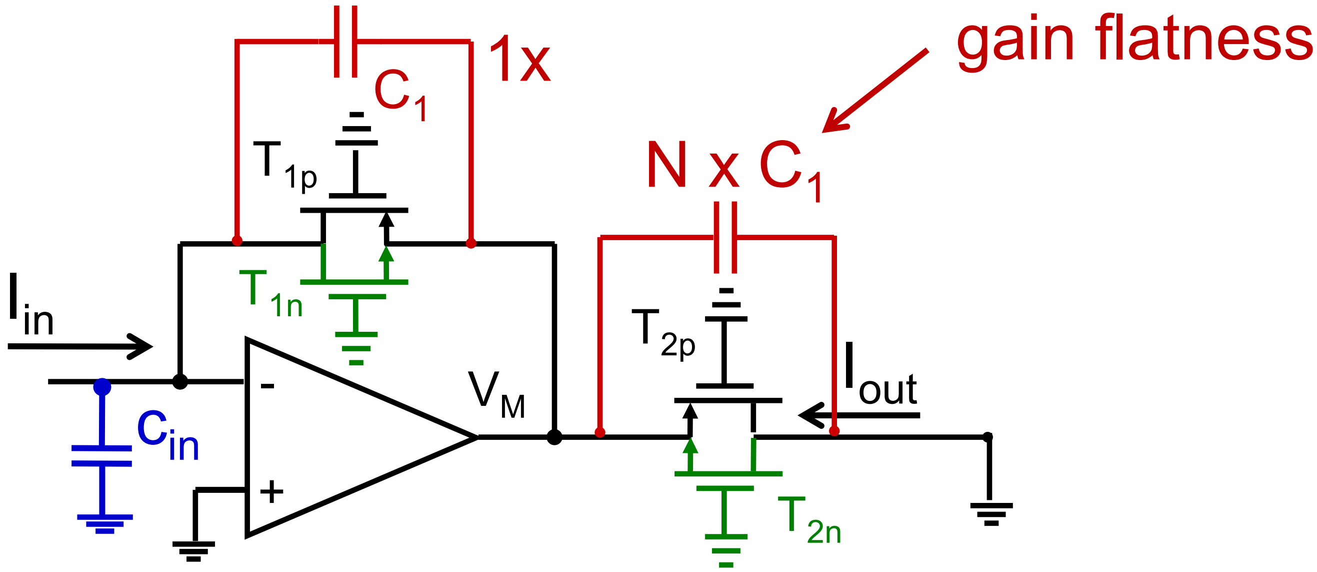
N replicas of M1
same bias condition

$I_{out} = N \times I_{in}$

Current amplification by matched MOSFETs

G. Ferrari, et al., *Electron. Lett.* **45** (2009) 1278-1280

Feedback stability and bidirectionality



$I_{in}>0$ → n-MOS
$I_{in}<0$ → p-MOS

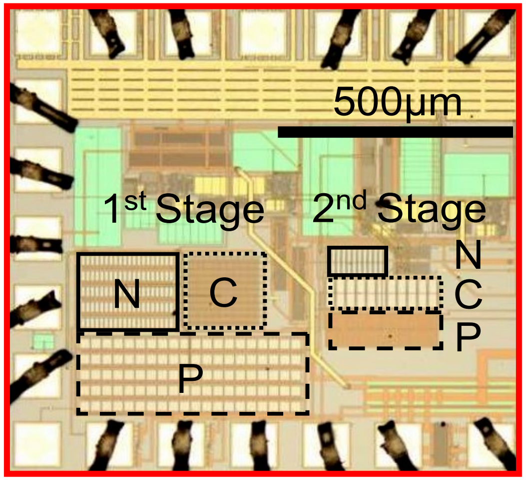
nMOS-pMOS matching better than 1%
(non-minimal transistor size)

$$loop\ gain \approx A_{OP}(s)\frac{g_m}{sC_{in}}$$

C_1 for feedback stability

$$loop\ gain \approx A_{OP}(s)\frac{C_1}{C_{in}+C_1}$$

CMOS implementation

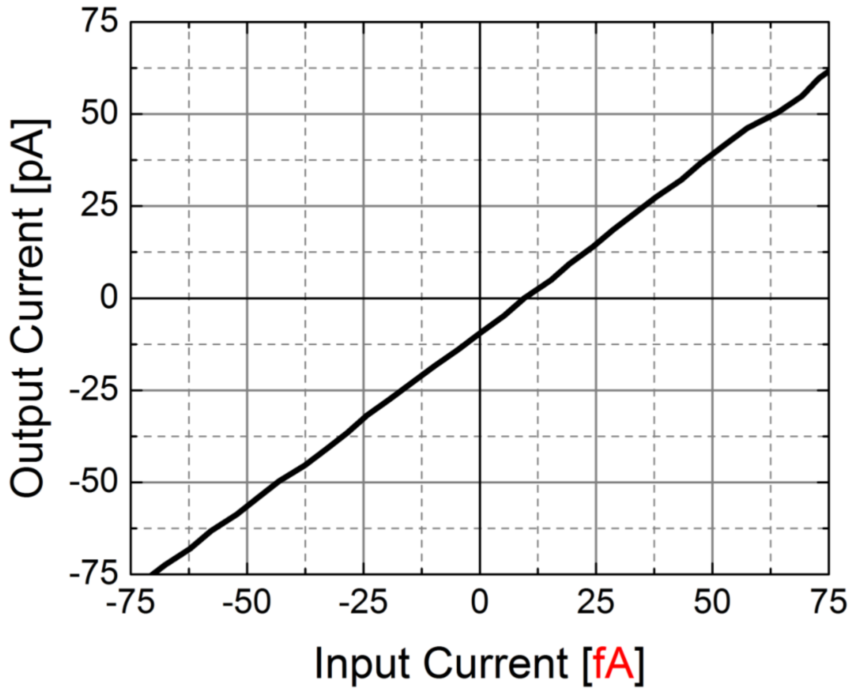


AMS 0.35µm, Area = 0.48mm²

Two stages:

99x10 = 990 total gain

V_{supply} = ±1.5V I_{bias} = 20mA
→ battery

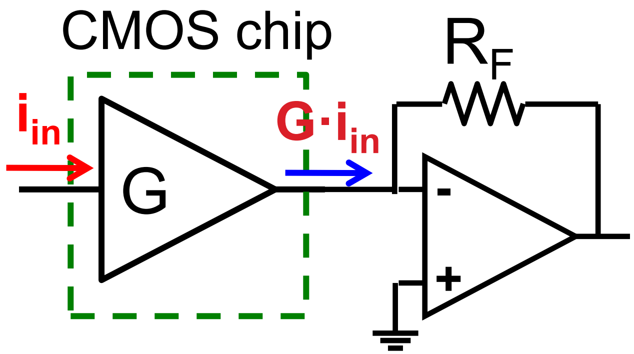


- Linearity error < 1%
- Current offset of 12fA
- femtoAmpere capability
- Bandwidth: DC – 1MHz

G. Ferrari, et al., *Electron. Lett.* **45** (2009) 1278-1280

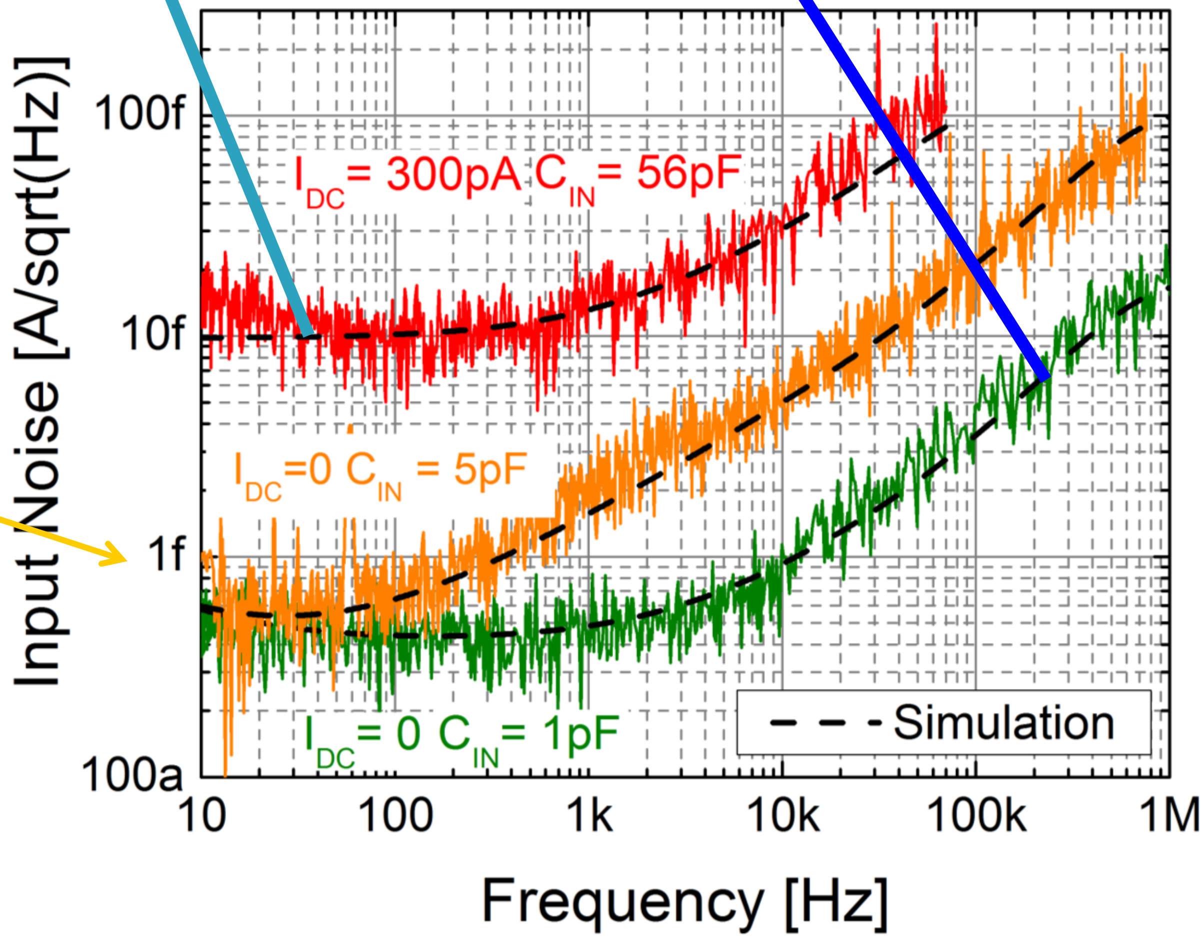
Noise Spectra

$$\overline{i_{TOT}^2} \cong \frac{4kT}{R_F G^2} + 2qI_{IN} + \overline{e_n^2} \cdot (2\pi f)^2 \cdot (C_{IN} + C_1)^2$$

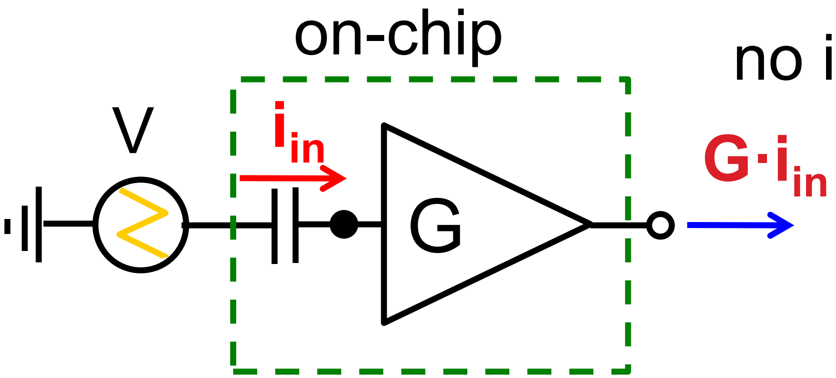


Equivalent to a **100GΩ** resistor!

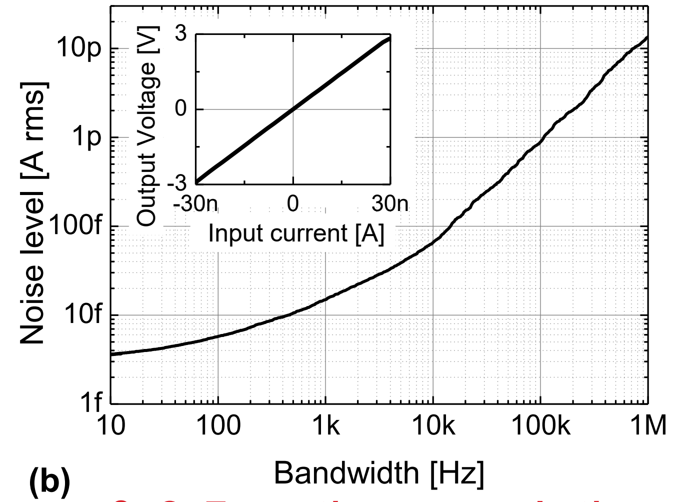
Limited by the external transimpedance (100kΩ)



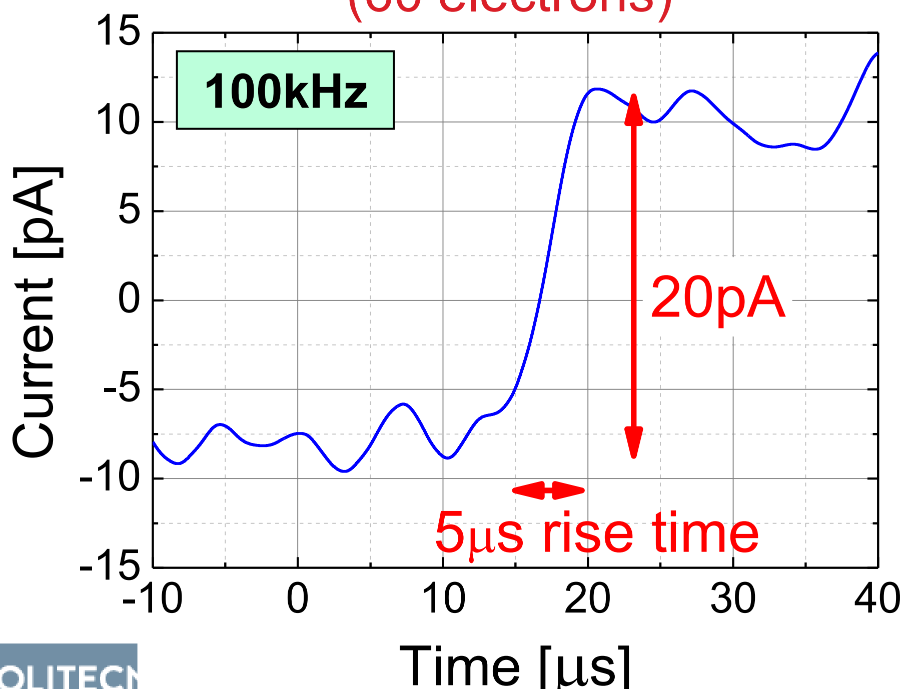
Low-Noise Current Tracking



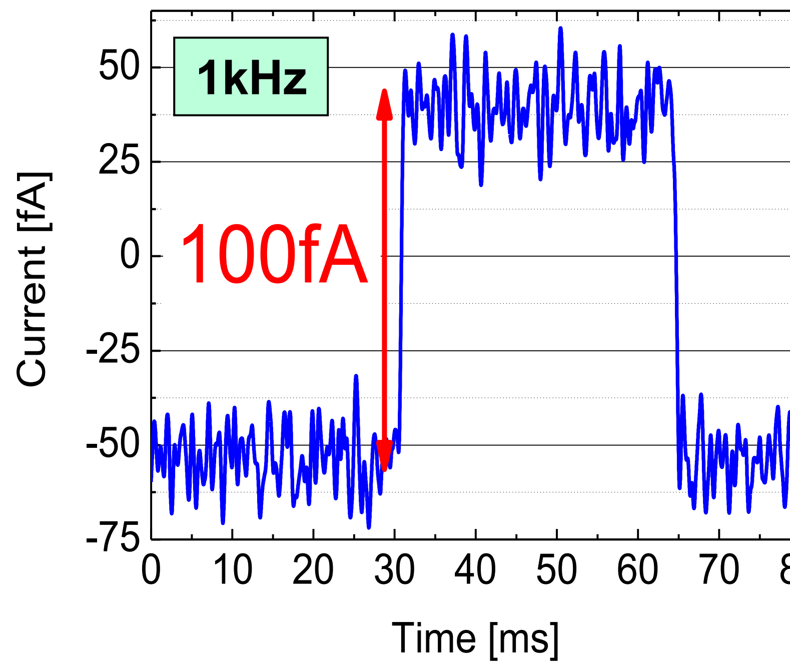
no input cable



1pA rms & 5µs time resolution (60 electrons)

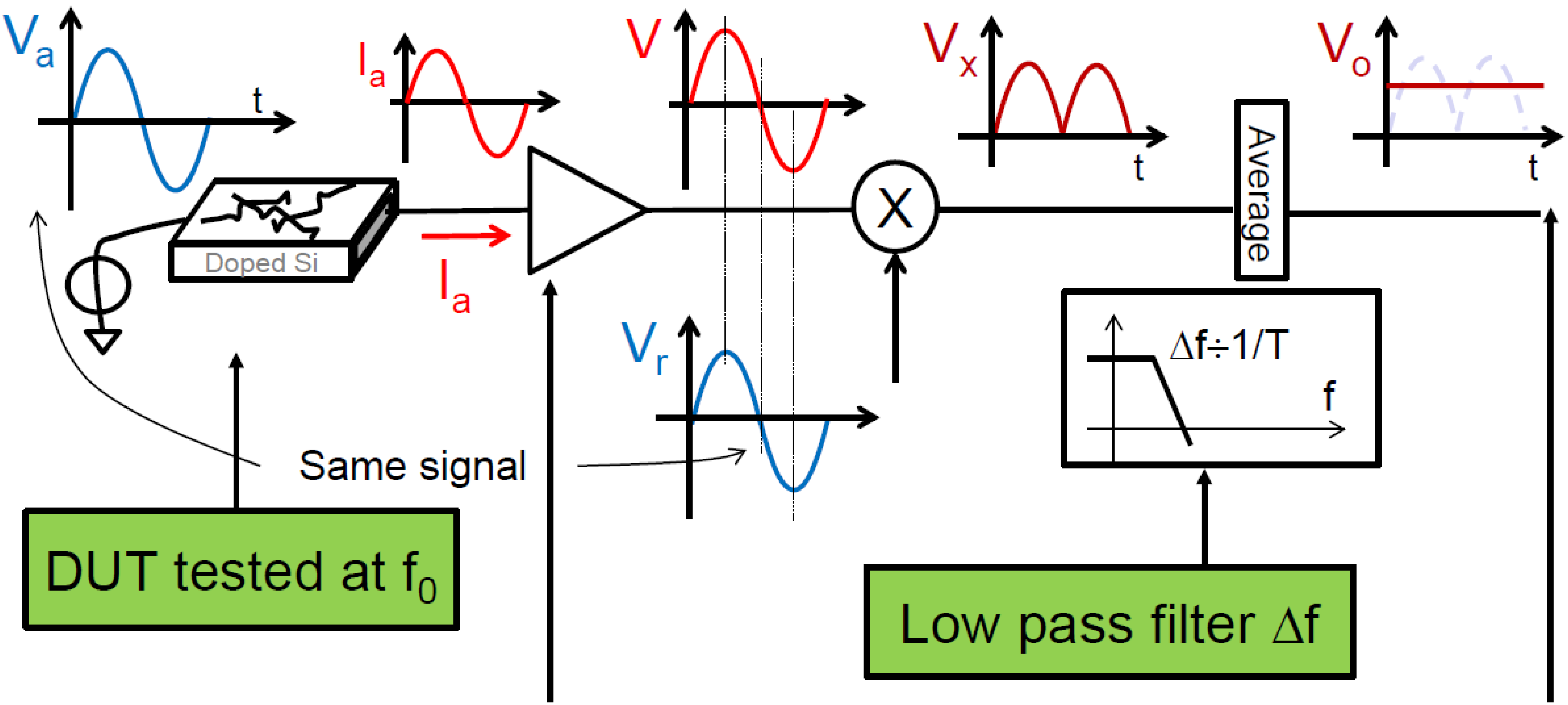


15fA rms & 0.5ms time resolution



The LOCK-IN idea

Lesson of Sampietro

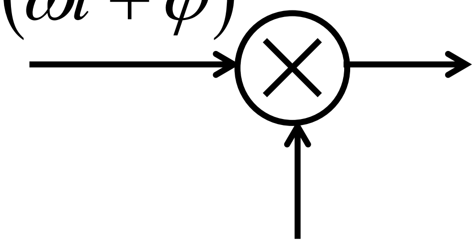


Is it possible to integrate a lock-in amplifier into a single chip?

Credited to Robert Dicke, founder of Princeton Applied Research (PAR) in the 1960's.

Multiplier

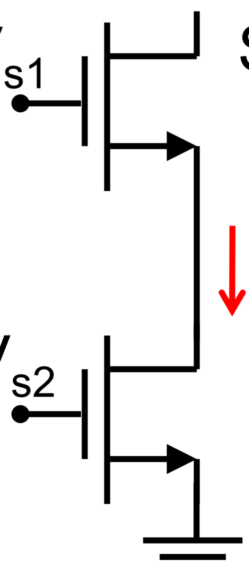
$$\alpha \cos(\omega t + \varphi)$$



$$\cos \omega t$$

$$\frac{1}{2}\alpha \cos\varphi + \frac{1}{2}\alpha \cos(2\omega t + \varphi)$$

Analog active multiplier

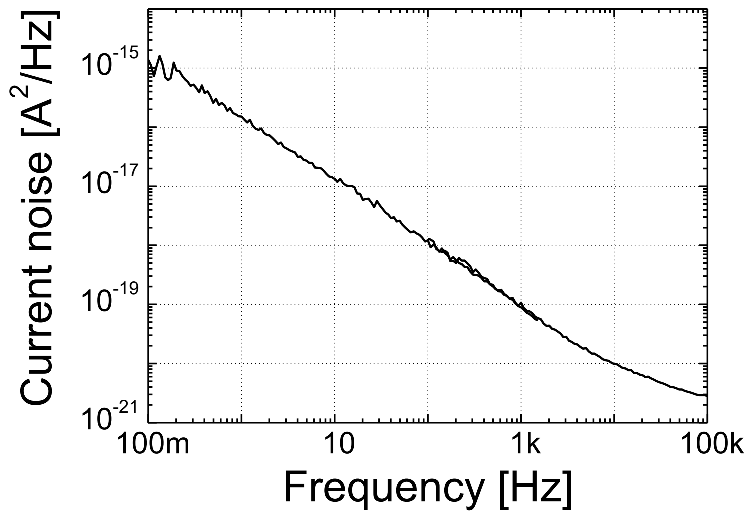


Saturation (follower)

$I_d = 2 \cdot k \cdot V_{s1} \cdot V_{s2} + \ldots$

Ohmic regime:

$I_d = k(2 \cdot (V_{GS} - V_T) \cdot V_{DS} - V_{DS}^2)$

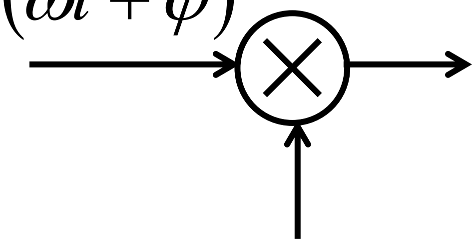


- High 1/f noise of CMOS
- Operate with small signals

"Small" SNR

Multiplier

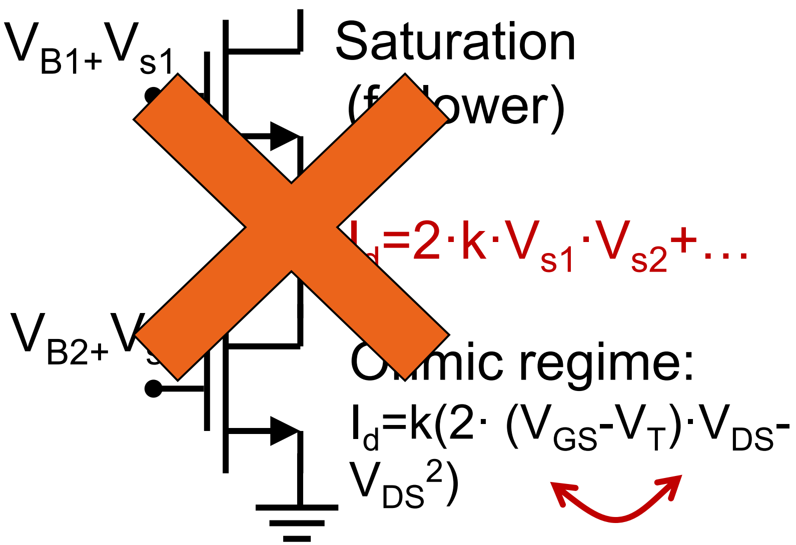
$\alpha\cos(\omega t+\varphi)$



$\cos\omega t$

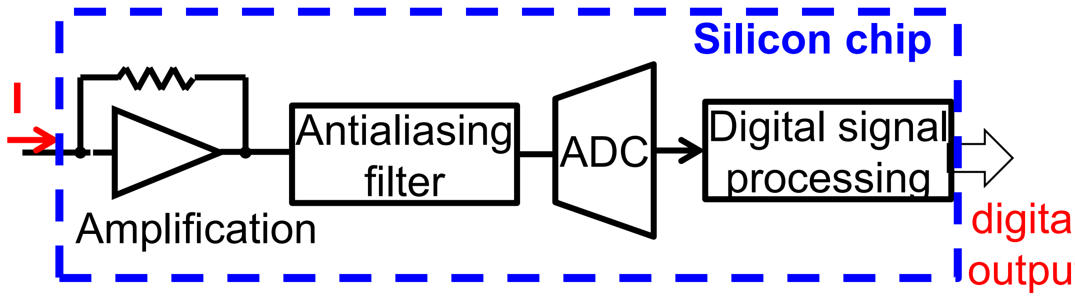
$$\frac{1}{2}\alpha\cos\varphi+\frac{1}{2}\alpha\cos(2\omega t+\varphi)$$

Analog active multiplier



Avoid if possible

Digital multiplier

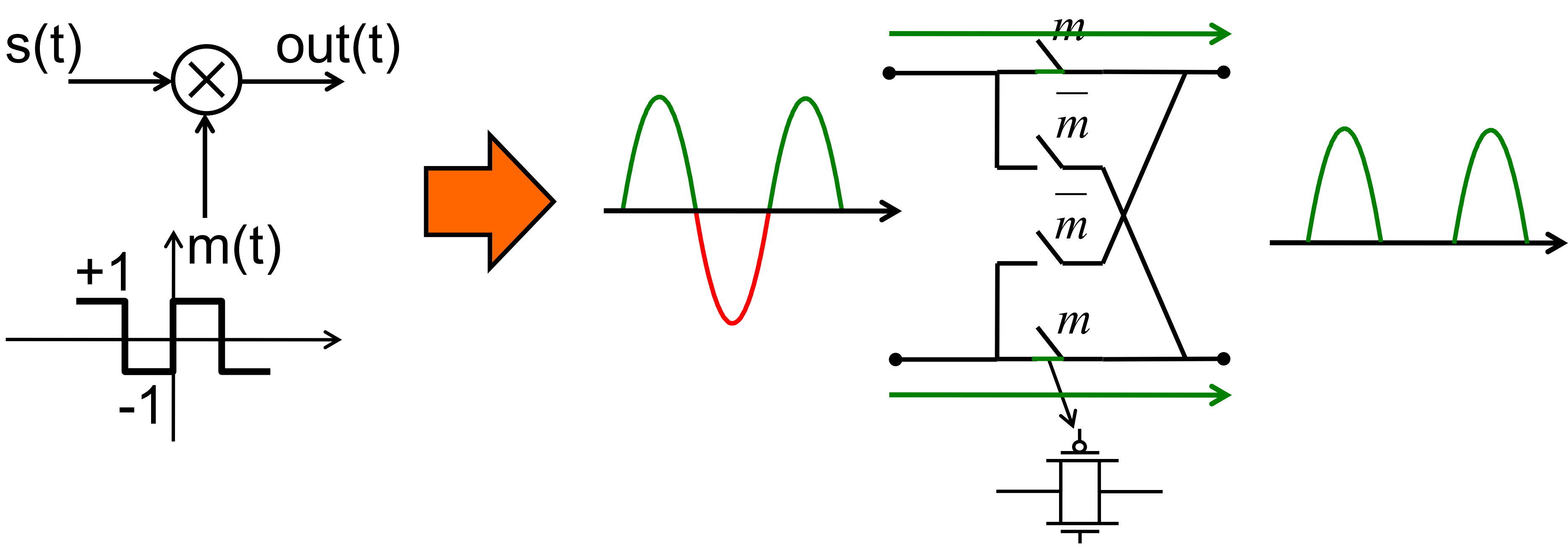


+ flexibility
- high speed ADC
- high speed DSP

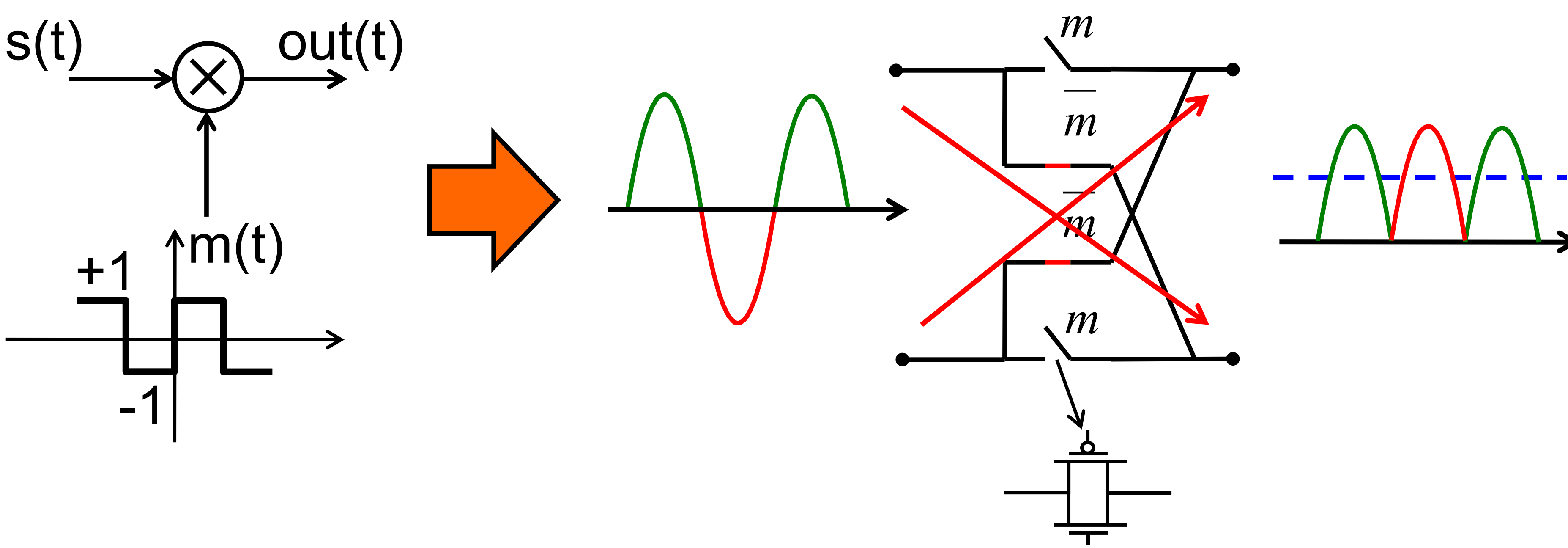
- Complexity
- Power consumption
- “Digital noise”
- Trade-off on the CMOS tech.

Avoid if possible

Passive multiplier



Passive multiplier

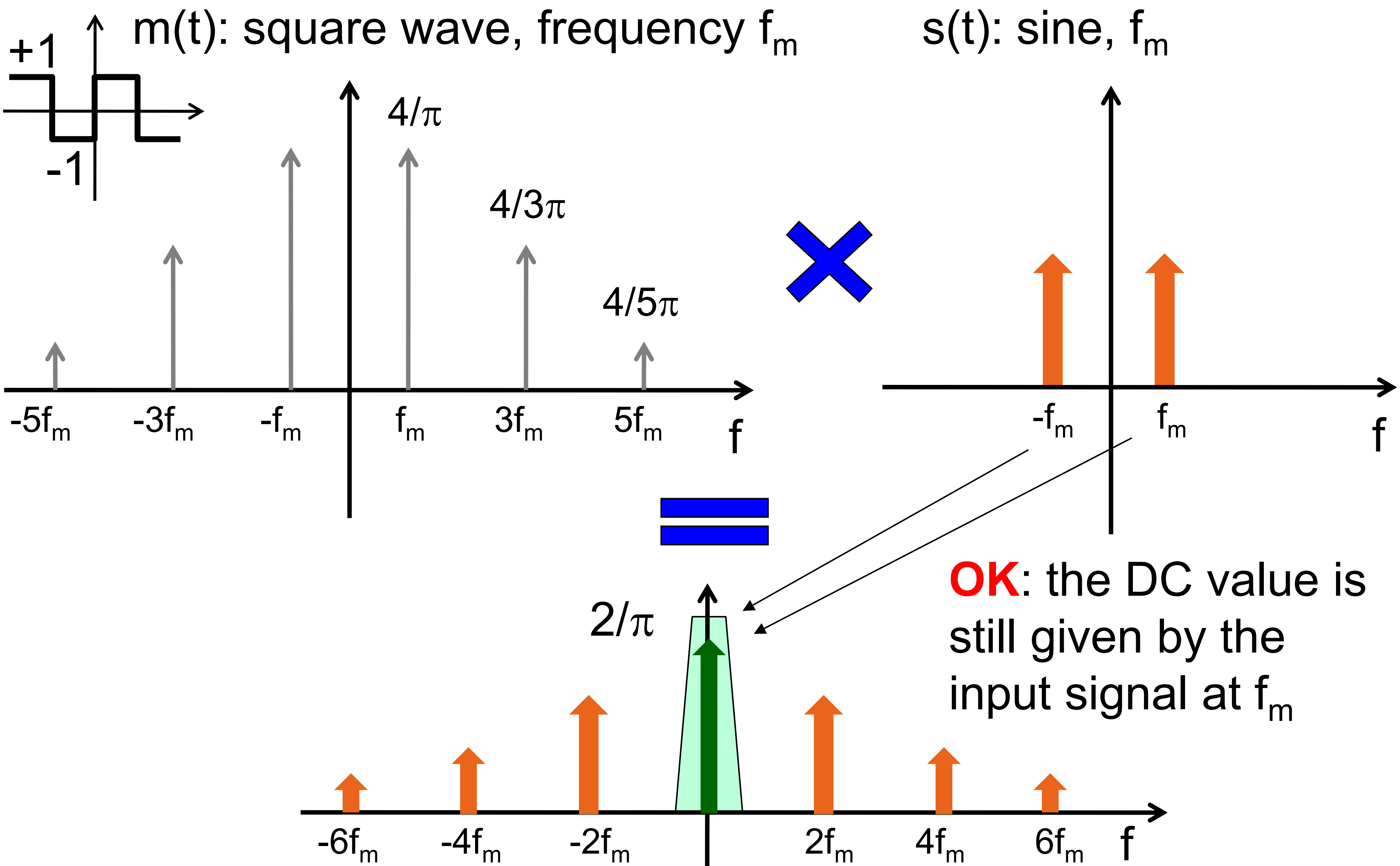


Rail-to-rail multiplier

MOSFET operating as switch, no (low) dc current bias

reduction of the flicker noise

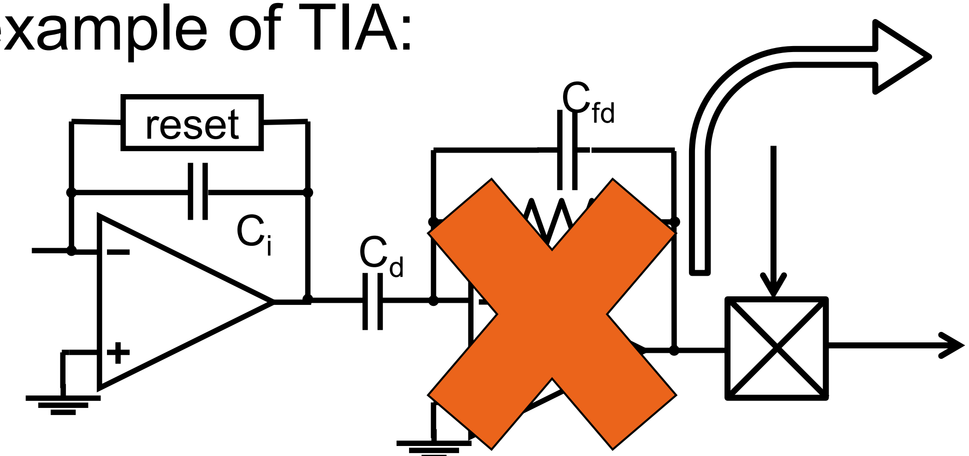
Frequency analysis - signal

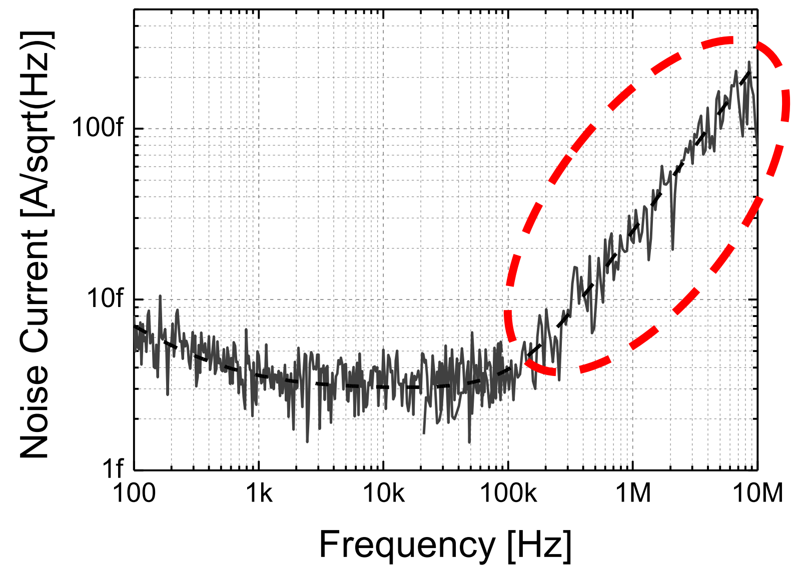


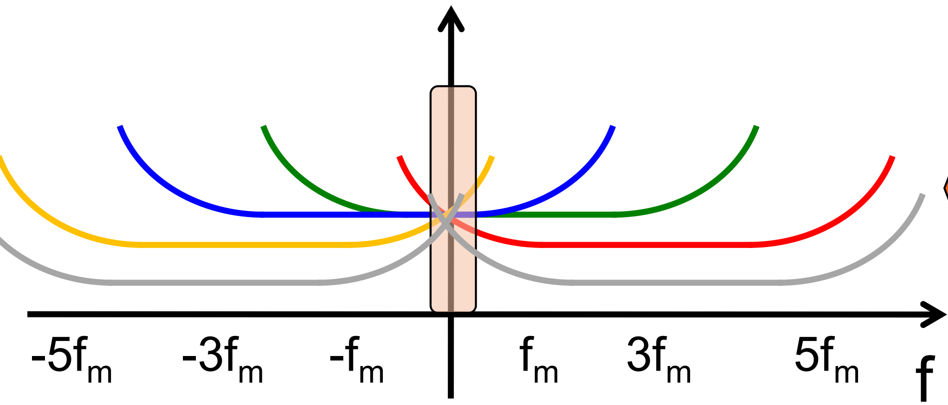
OK: the DC value is still given by the input signal at f_m

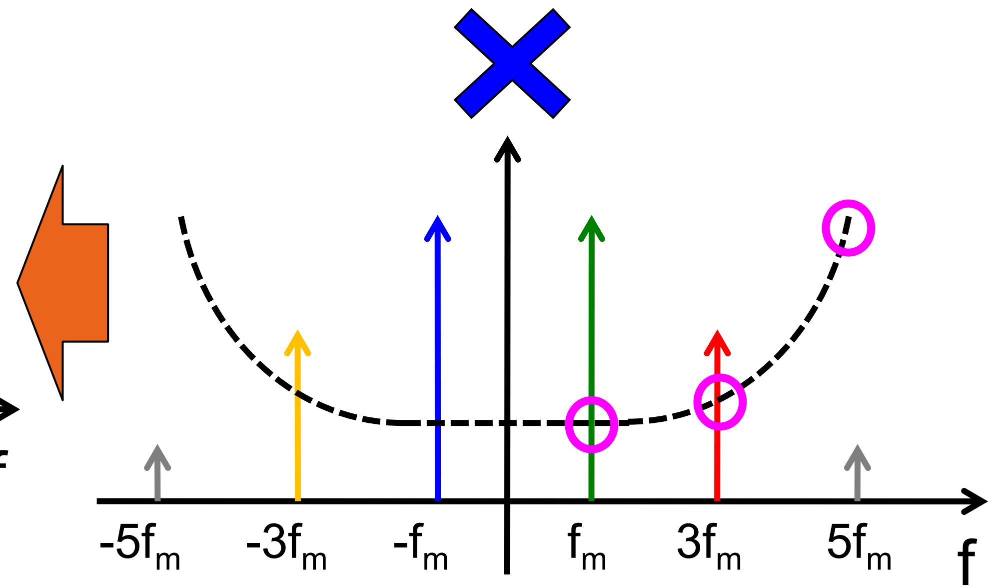
Frequency analysis - noise

example of TIA:



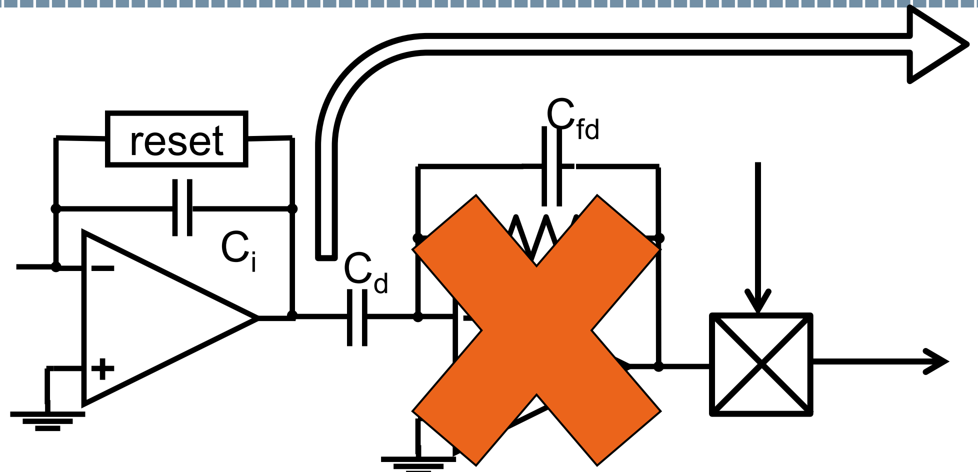


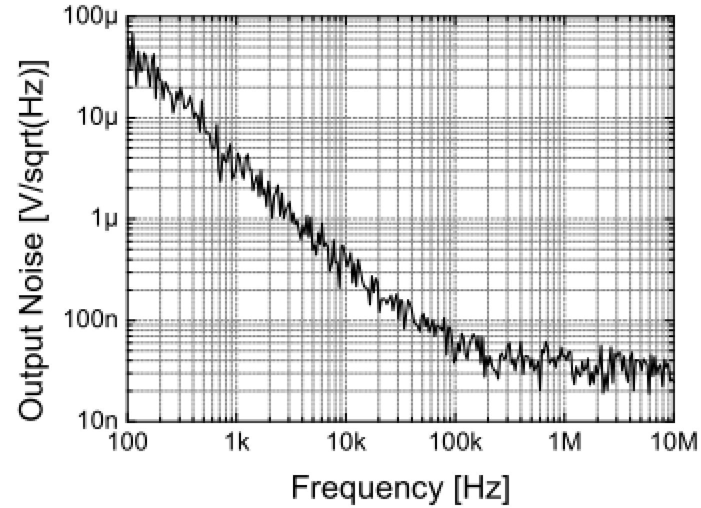


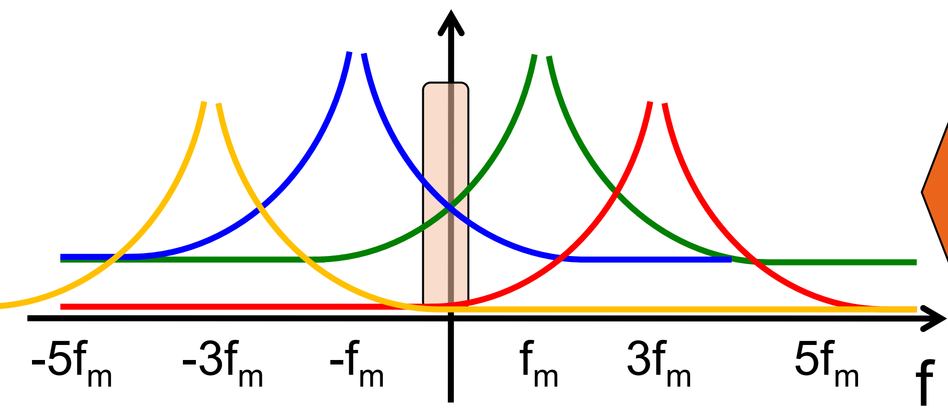


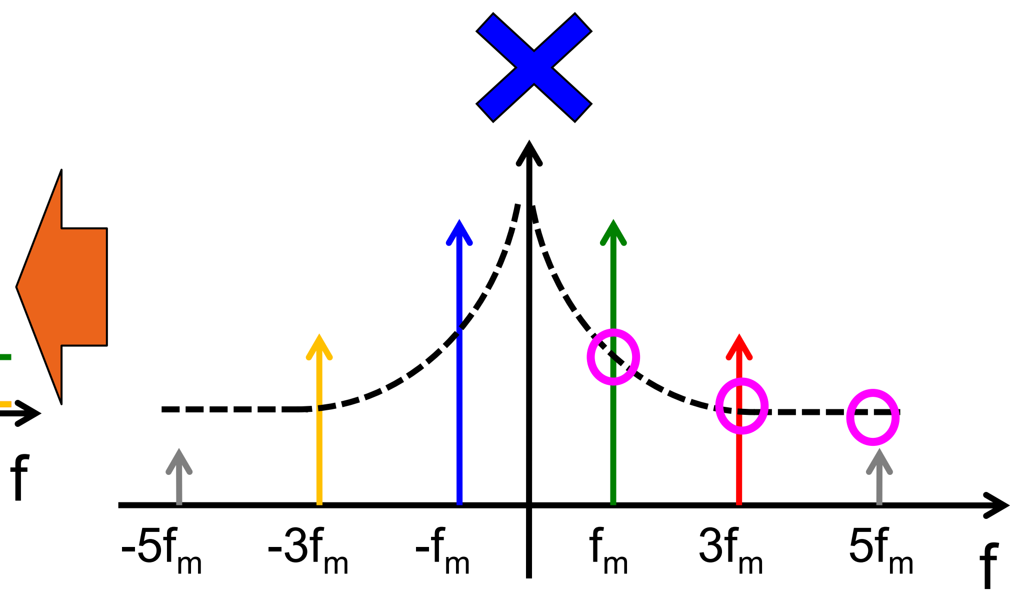
High frequency noise → DC!

Frequency analysis - noise



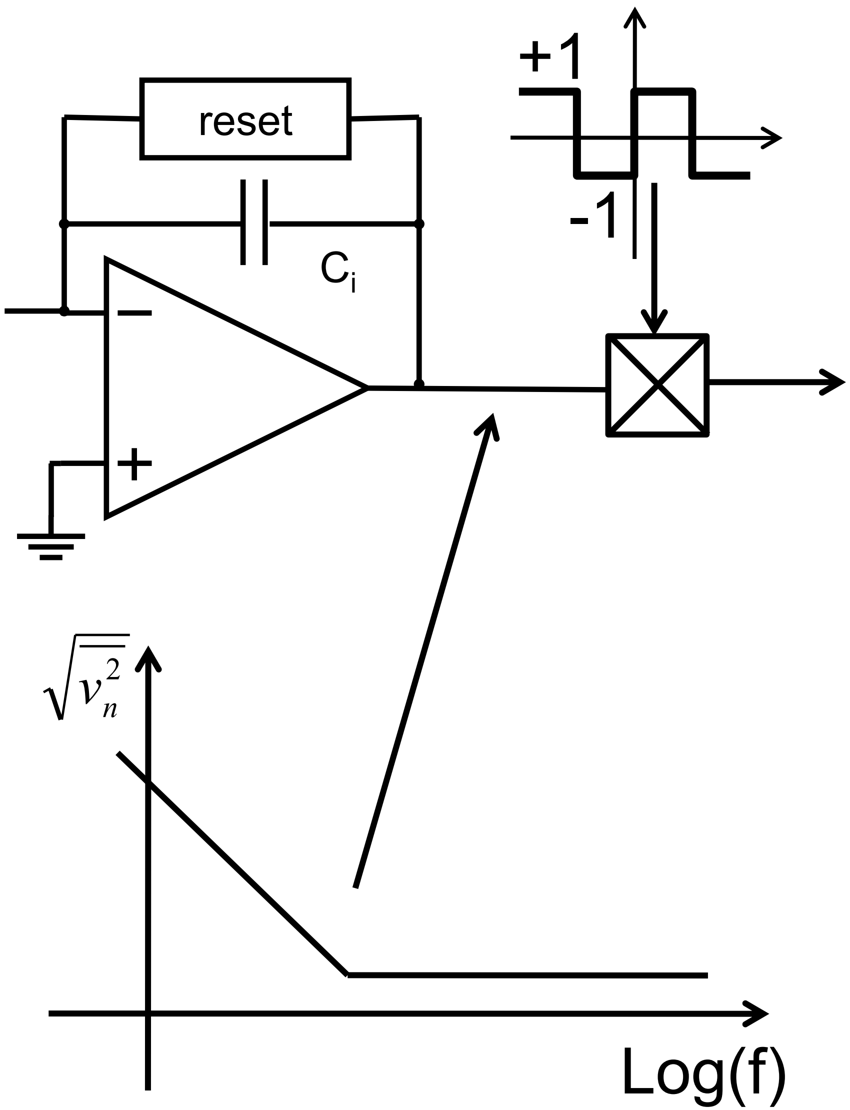






≈ noise of ideal multiplier

Simple integrated LIA

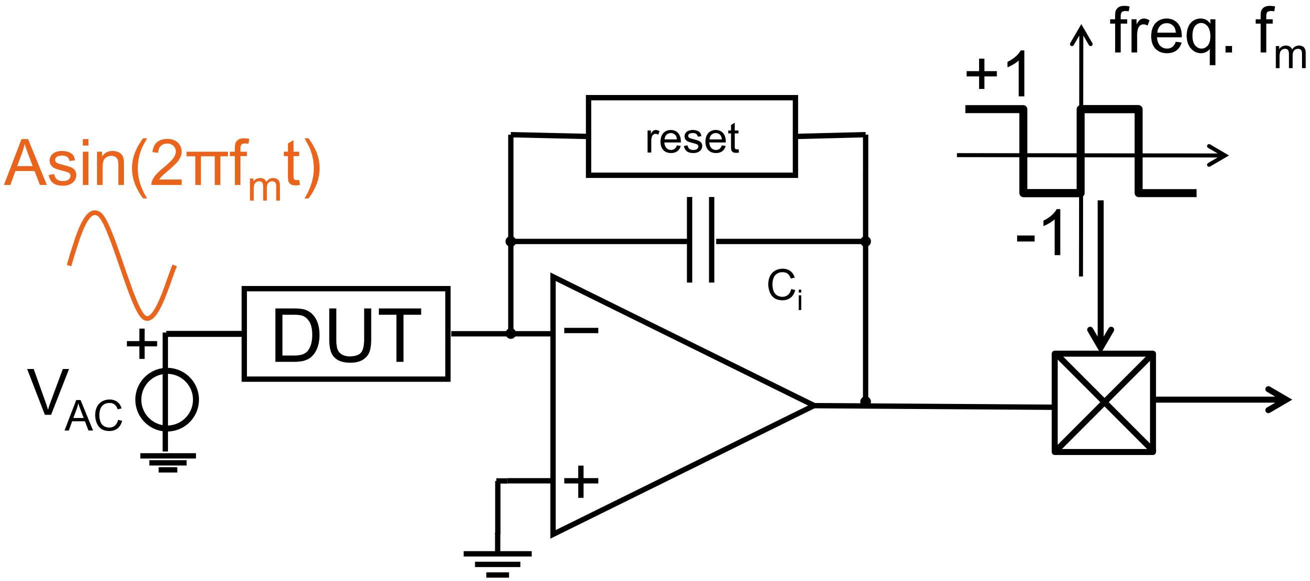


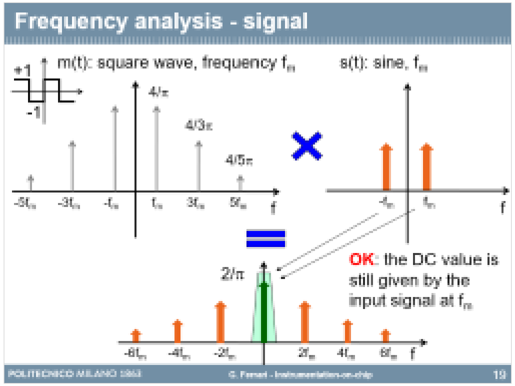
1. Passive multiplier
2. Keep a low HF noise

   maximum SNR reduced to 20% respect to an ideal multiplier ***OK***

3. Integrator: phase shift of 90°, easily compensated
4. Simple digital control of the multiplier
5. Used to limit the effect of 1/f noise (chopper amplifier)

Waveform at the input: sinewave

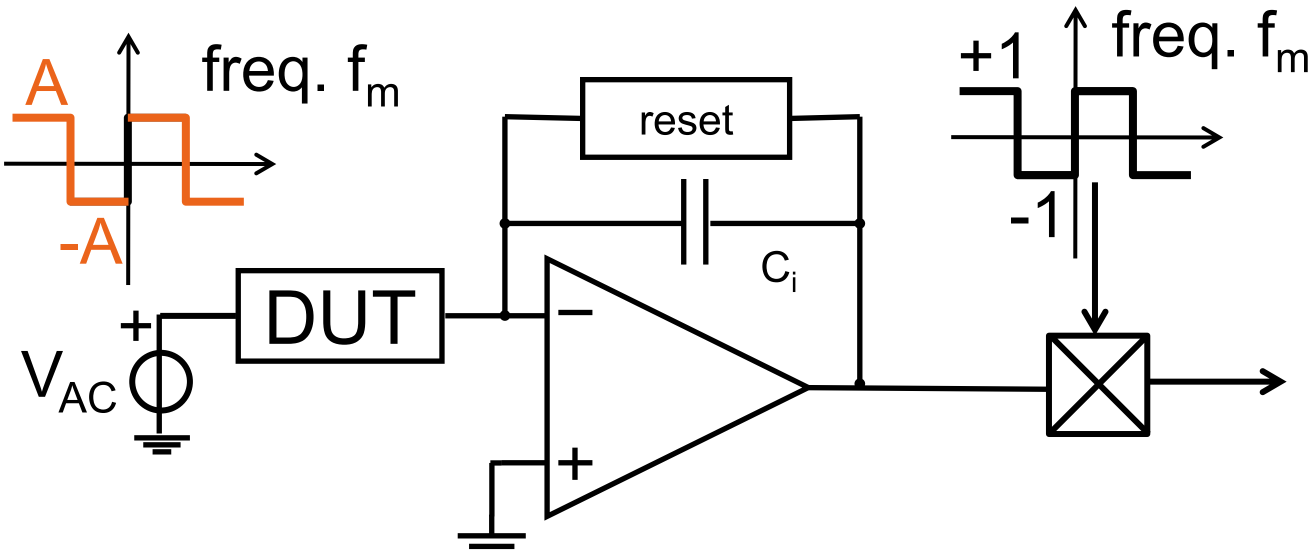




+ as in an ideal LIA the output is given by Z_{DUT} at f_m

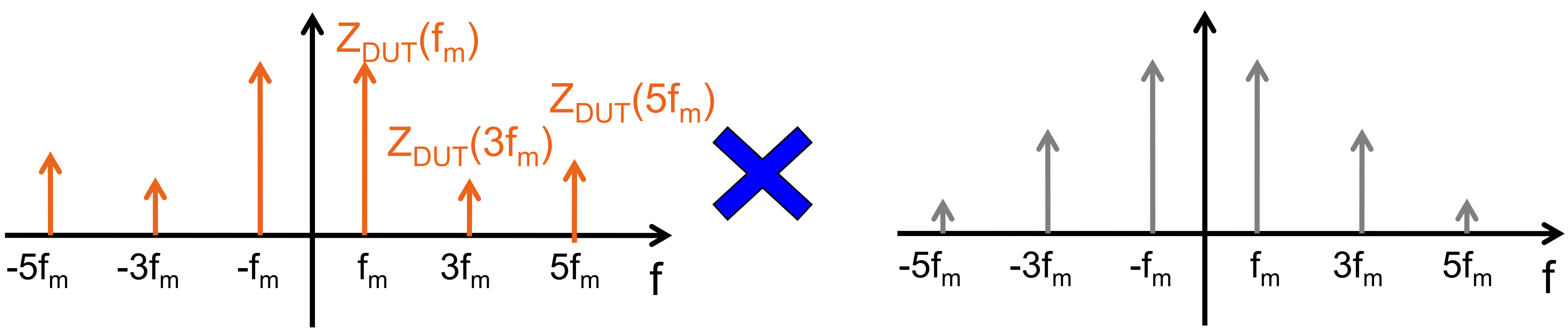
- complexity of the sinewave generation

Waveform at the input: squarewave



+ simple generation

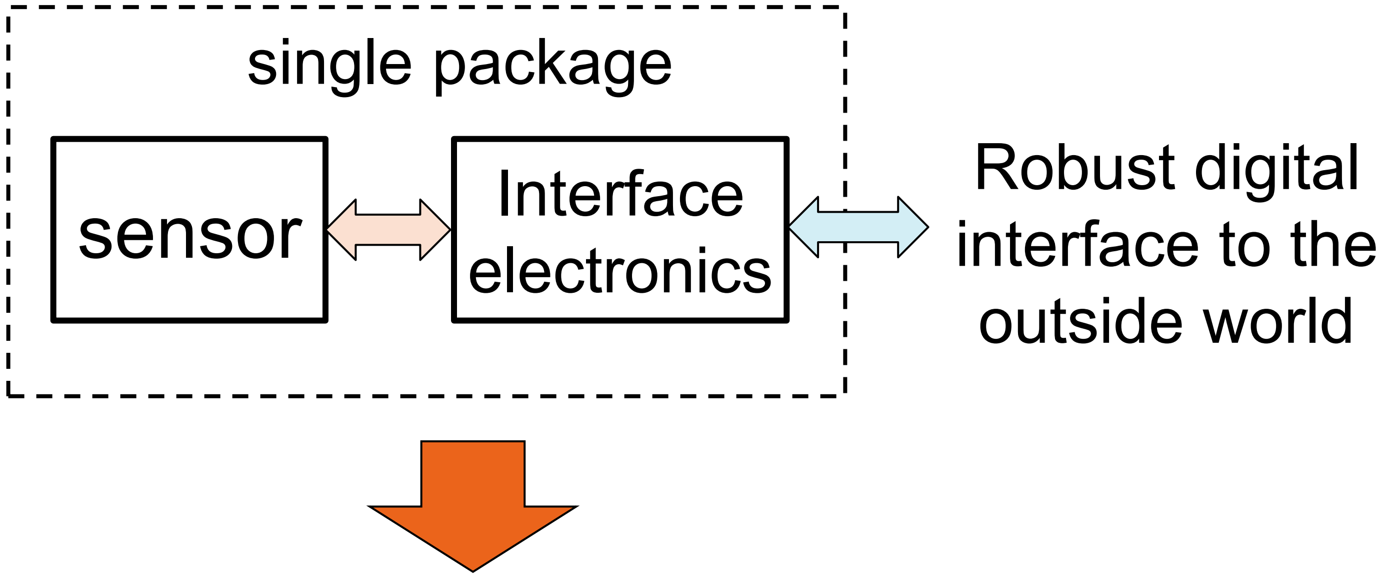
(digital signal, optical chopper,…)



- poor frequency selectivity: $Z_{DUT}(f_m)$, $Z_{DUT}(3f_m)$, $Z_{DUT}(5f_m)$,…
- no impedance spectroscopy
- OK for "pure" capacitive or resistive devices

A step further…

Smart Sensor System: sensor+electronics co-design and co-packaging



single chip combining sensor and electronics

- Light: CMOS imager
- Capacitance: fingerprint reader
- Temperature

MEMS technology:

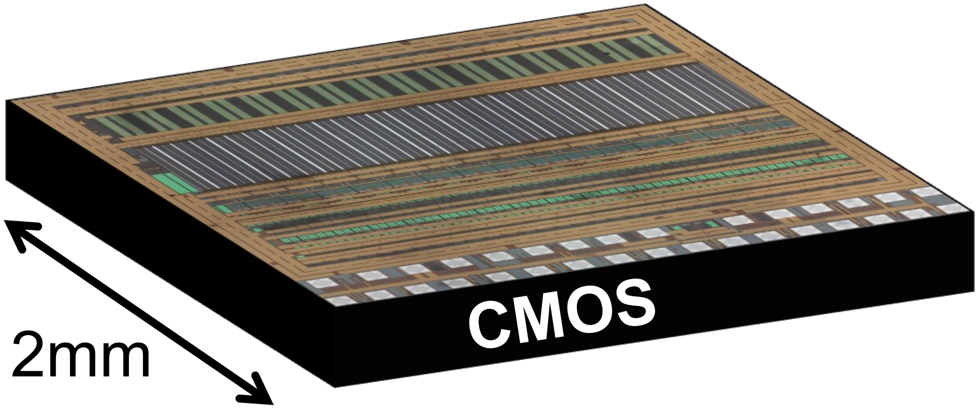
- Magnetic field: compass
- Force: accelerometer, gyroscope

Optimal sensor-electronics connection, multichannel

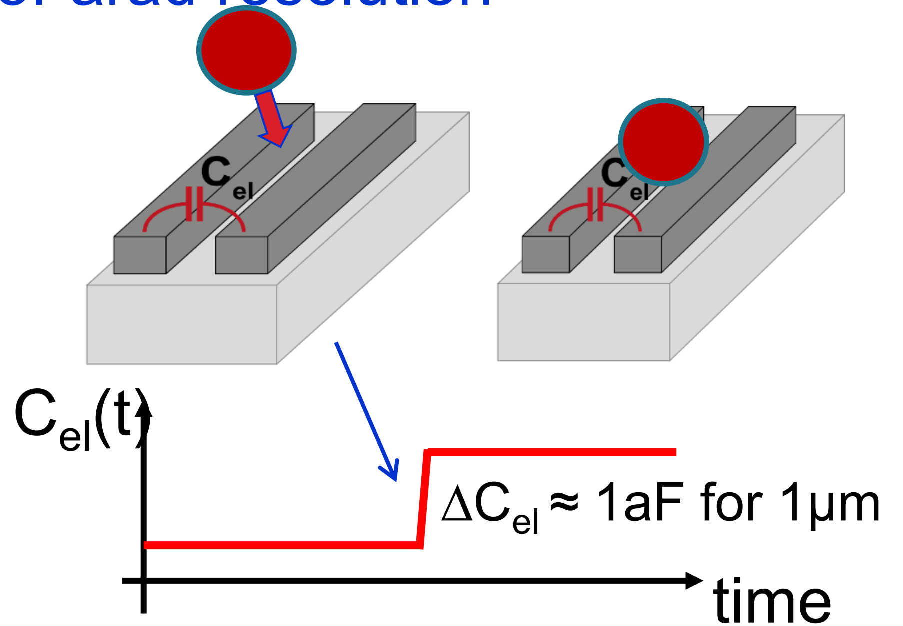
CMOS Particulate Matter detector:

- Compactness
- Low cost / mass production
- Scaled lithography for microelectrodes on chip
- Integrated electronics with ZeptoFarad resolution

See the lesson on differential measurements

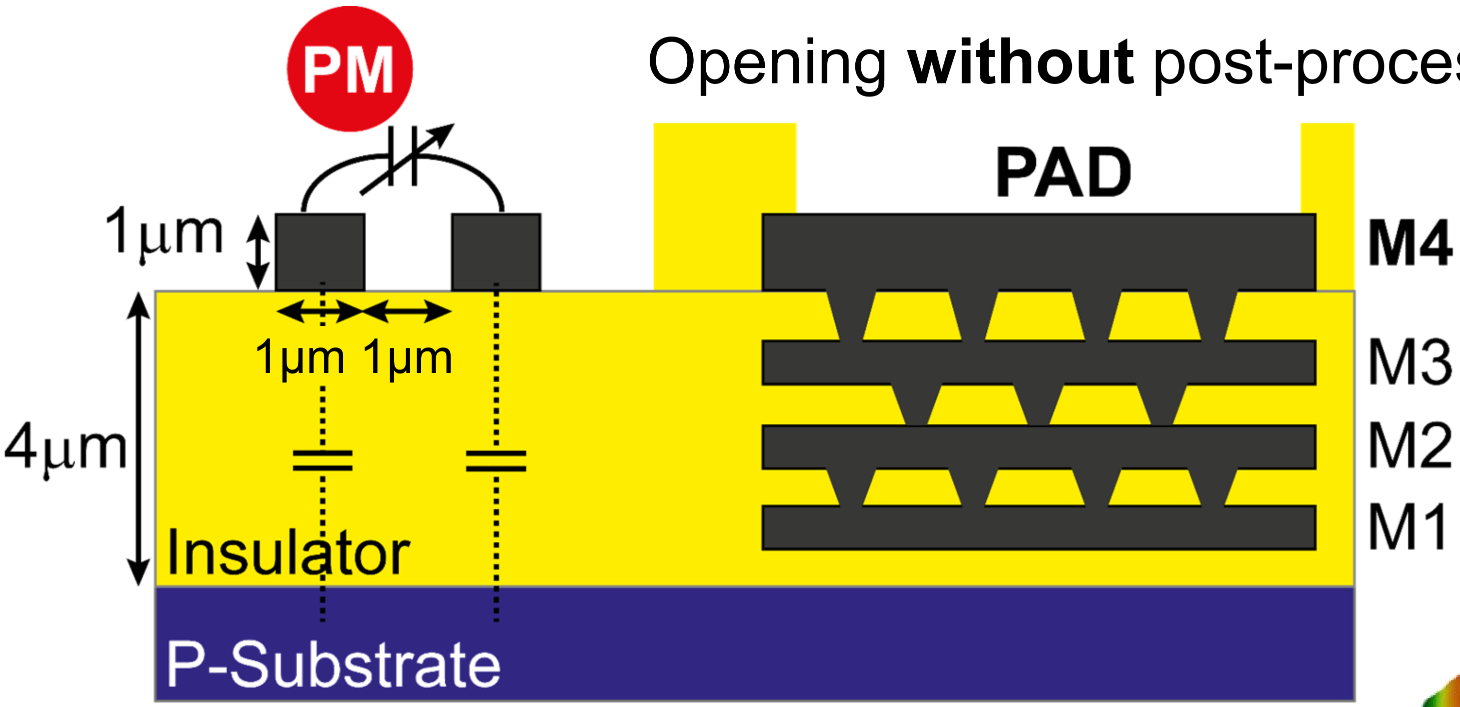


P. Ciccarella, et al., *IEEE JSSC* 2016



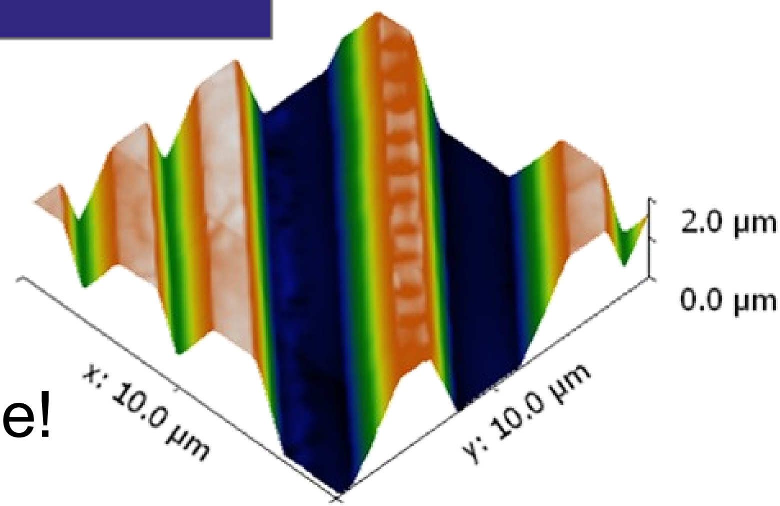
On-chip electrodes

Opening **without** post-processing steps



Top metal for electrodes fabrication

AFM Check



AMS 0.35µm standard CMOS technology

Electrodes on chip: stray cap. fF range!

Interdigitated Electrodes

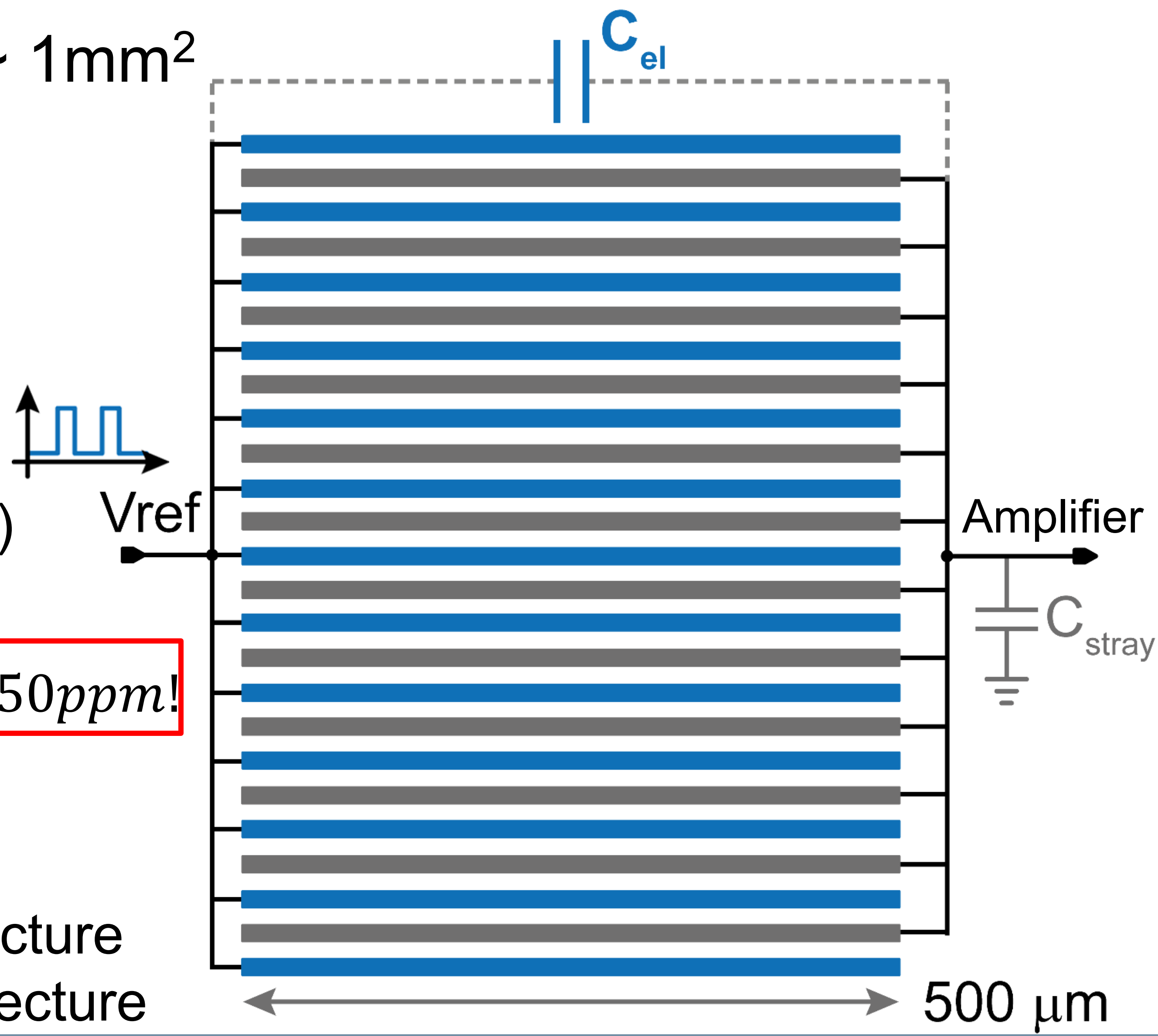
Sensitive area ~ $1mm^2$

Interdigitated structure

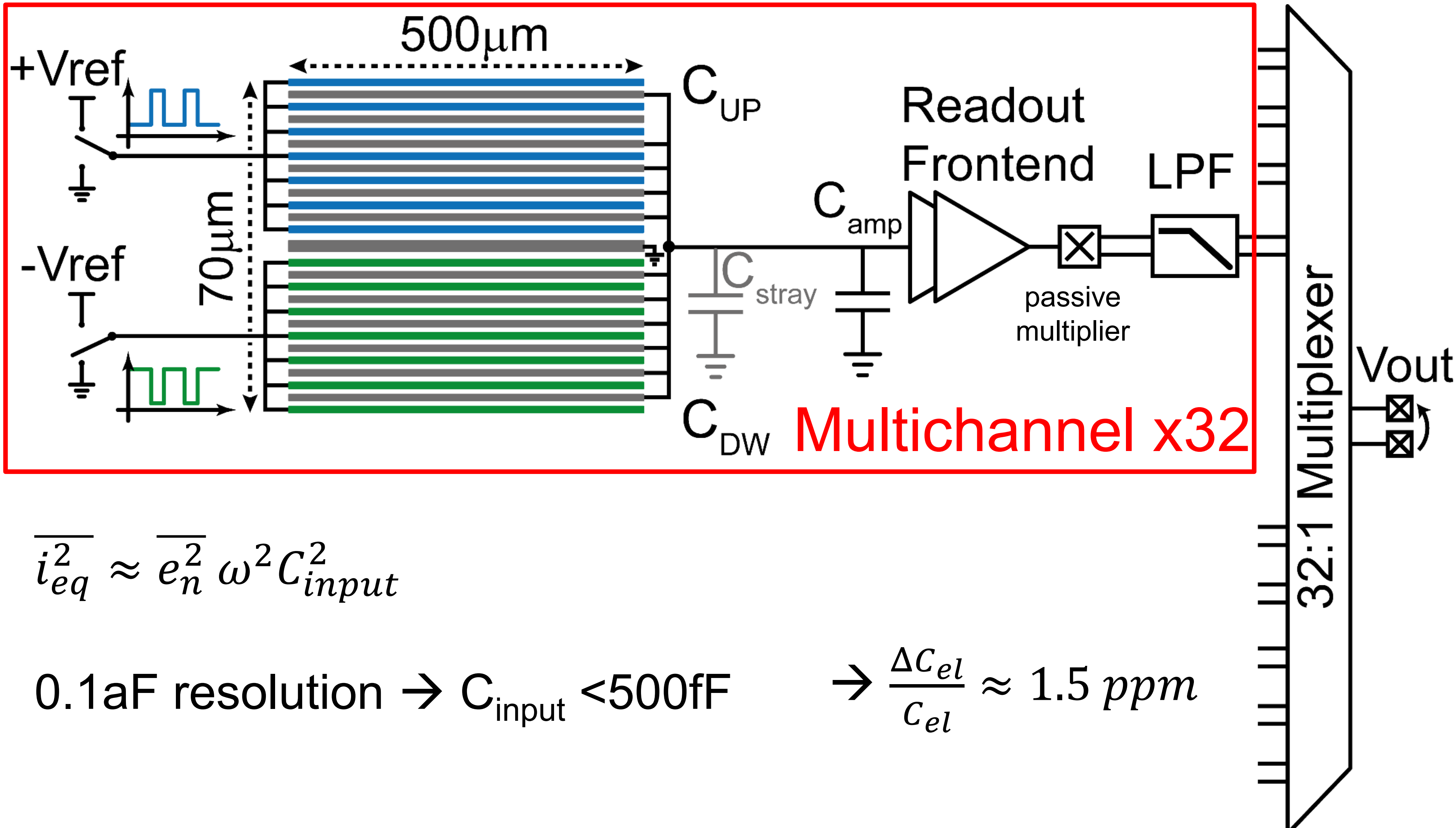
- C_{el} = 15pF
- ΔC = 700zF (1µm)

$$\frac{\Delta C_{el}}{C_{el}} = \frac{700zF}{15pF} \sim 0.050ppm!$$

Differential architecture
Multichannel architecture



Area-Resolution tradeoff

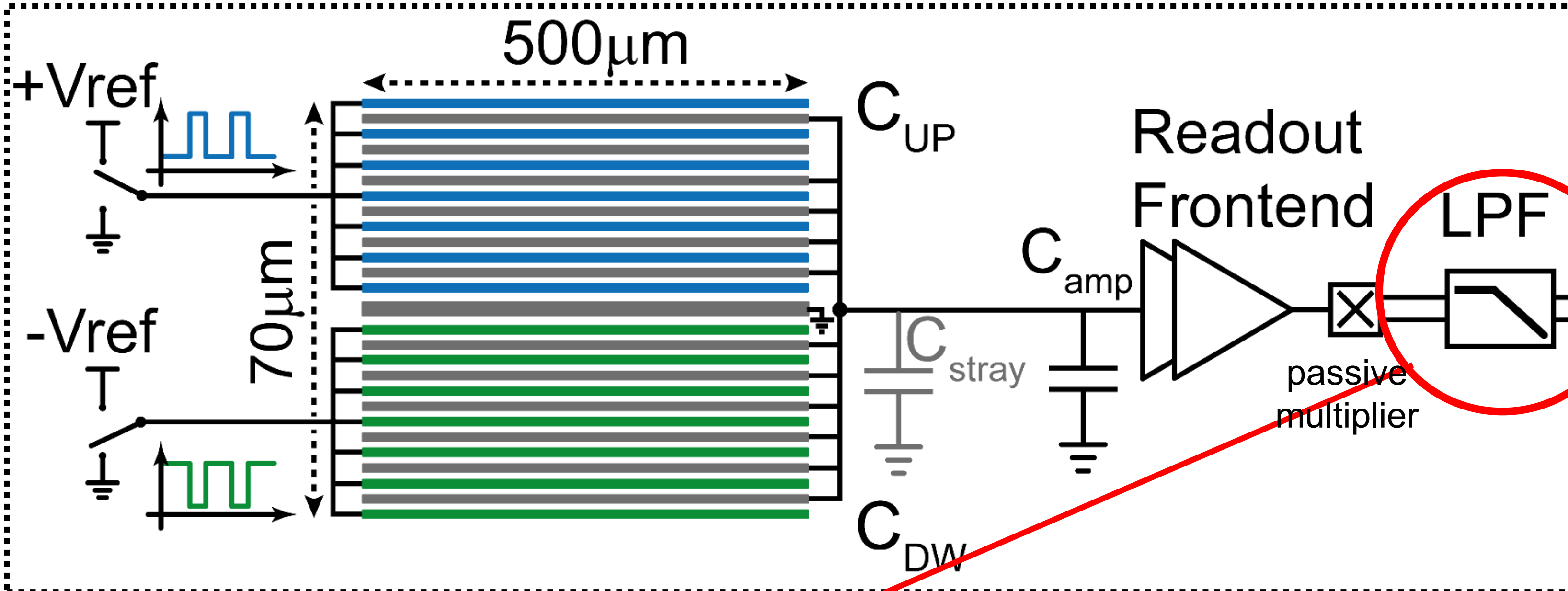


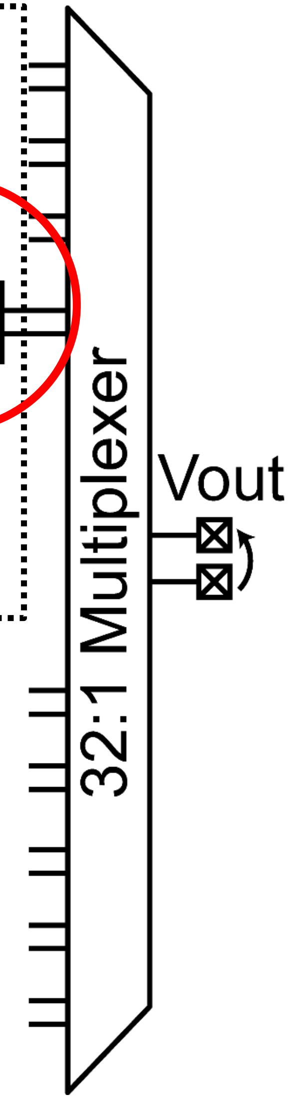
$$\overline{i_{eq}^2} \approx \overline{e_n^2}\,\omega^2 C_{input}^2$$

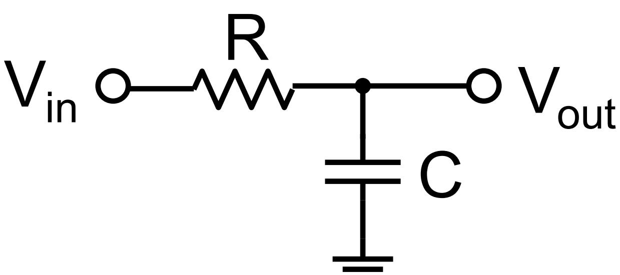
0.1aF resolution → C_{input} <500fF → $\frac{\Delta C_{el}}{C_{el}} \approx 1.5\ ppm$

→ 32 diff. channels (Amp+LIA+Filters) for 1mm² sensitive area

Low pass filter







C is limited to a few pF

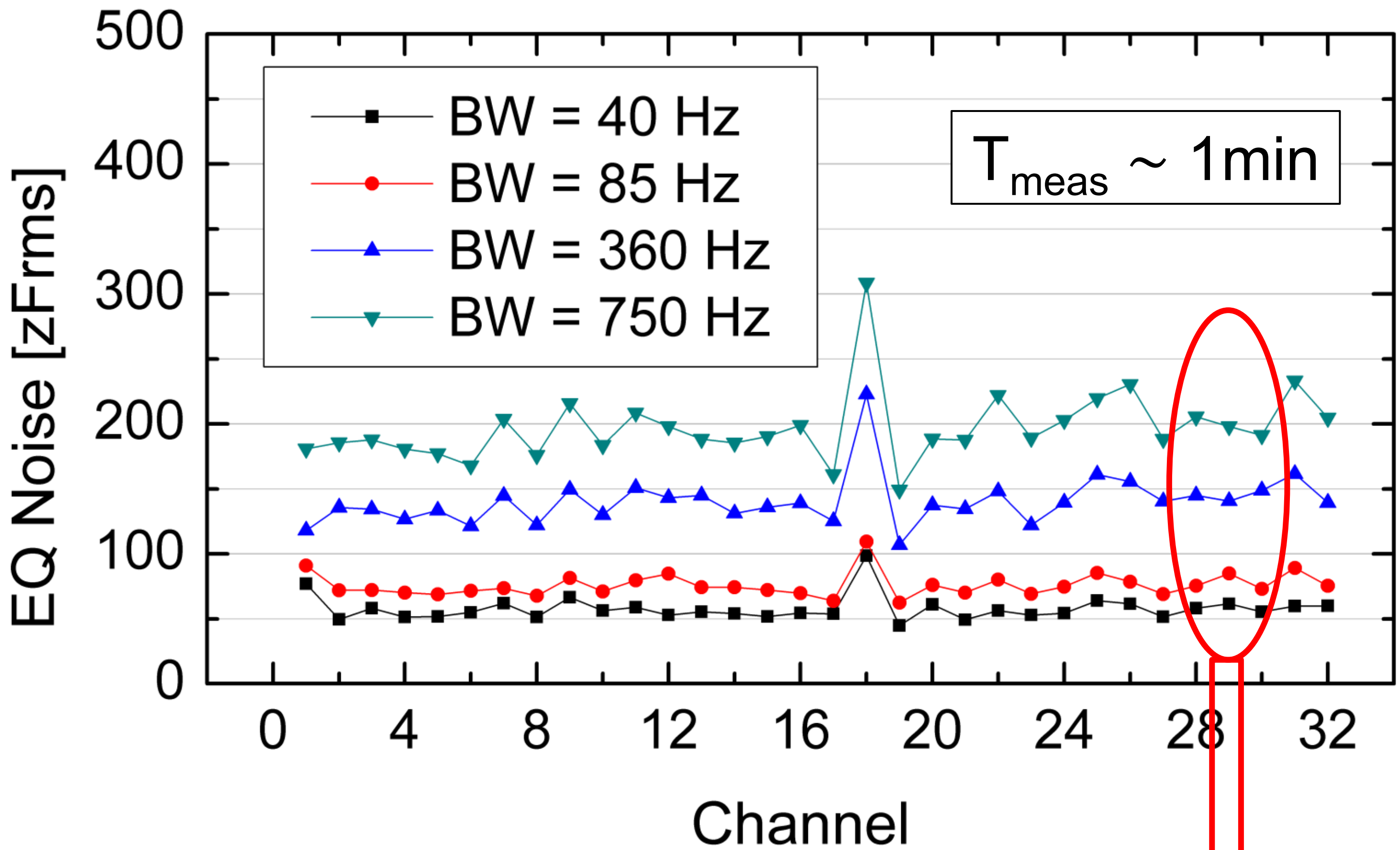
CMOS filters are noisy!
(≈ 60μV @ 1pF)

High gain before the filters!

Noise of the RC filter:

$$\overline{N^2} = \int_0^{+\infty} \frac{4kTR}{|1+\omega^2 R^2 C^2|} d\omega = \frac{kT}{C}$$

Measured Capacitive Noise

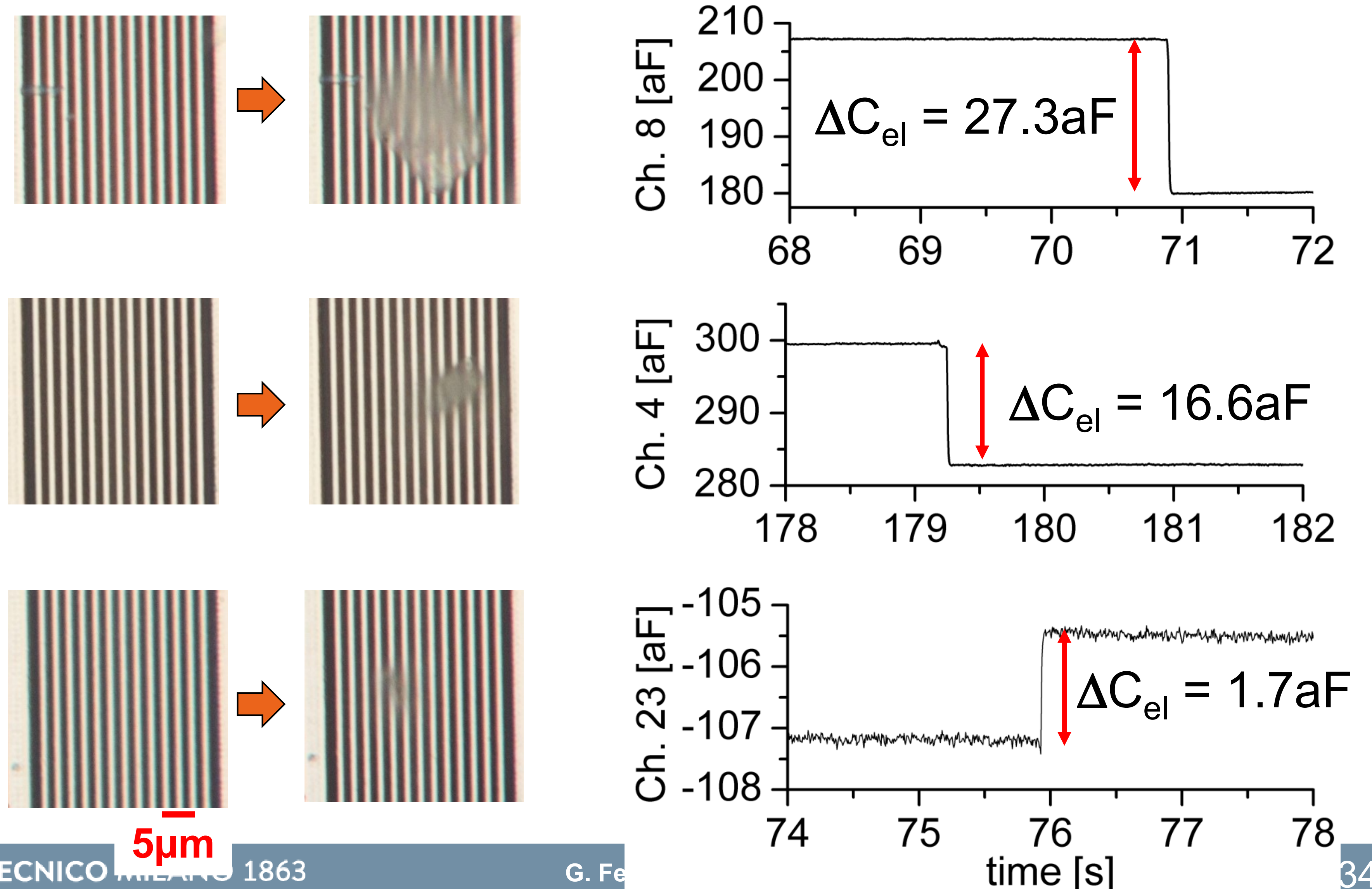


- 65zF rms Average Noise (BW = 40Hz)
- Noise $\propto \sqrt{BW}$

Exp. Results: PM Detection Examples

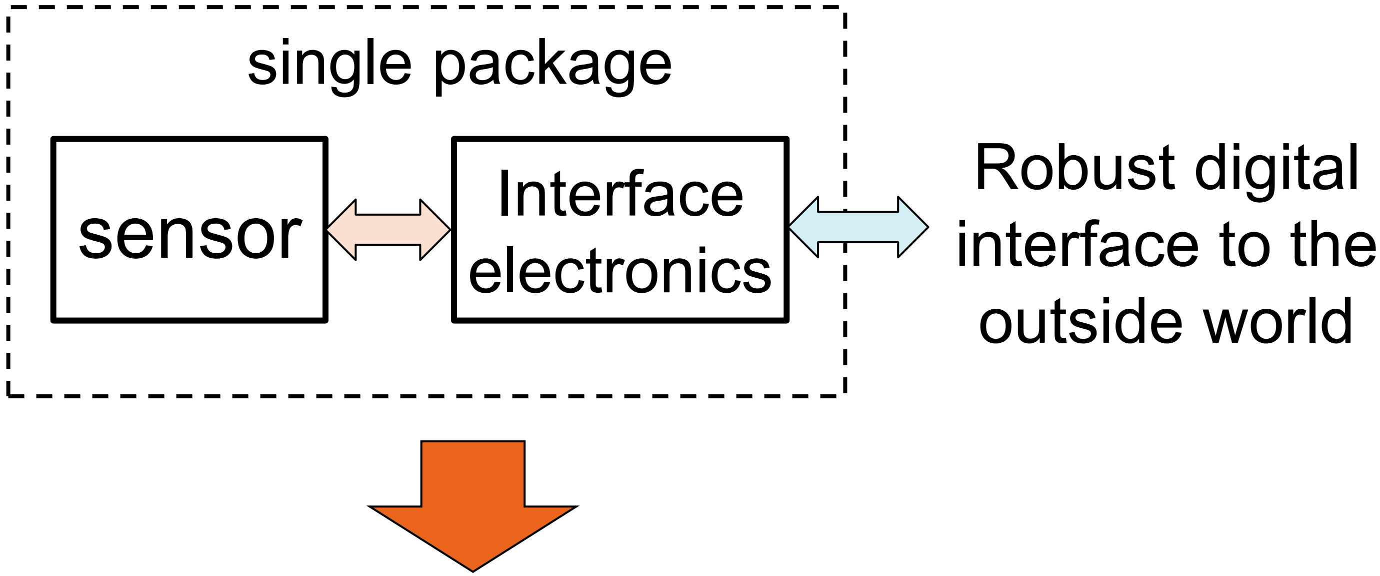
- Single talc particle deposition ($\varepsilon_r = 2.4$)

P. Ciccarella, et al., *IEEE JSSC* 2016



A step further…

Smart Sensor System: sensor+electronics co-design



single chip combining sensor and electronics

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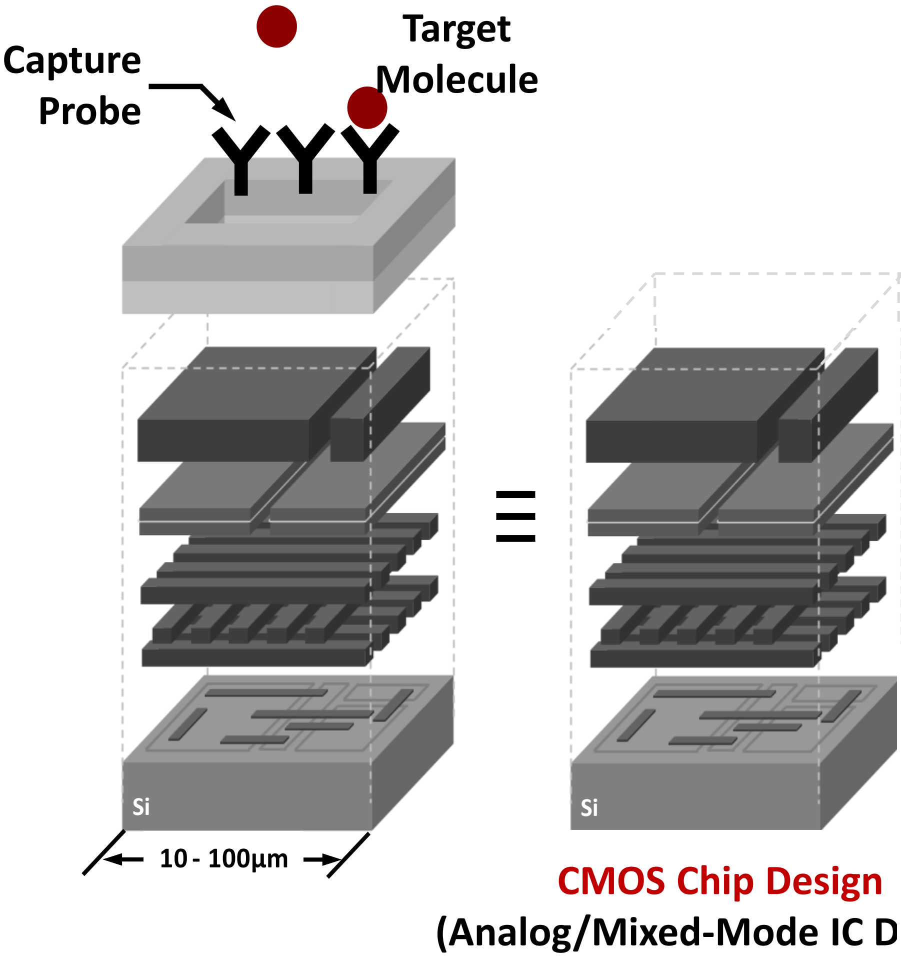
MEMS technology:

- Magnetic field: compass
- Force: accelerometer, gyroscope

Biosensor ?

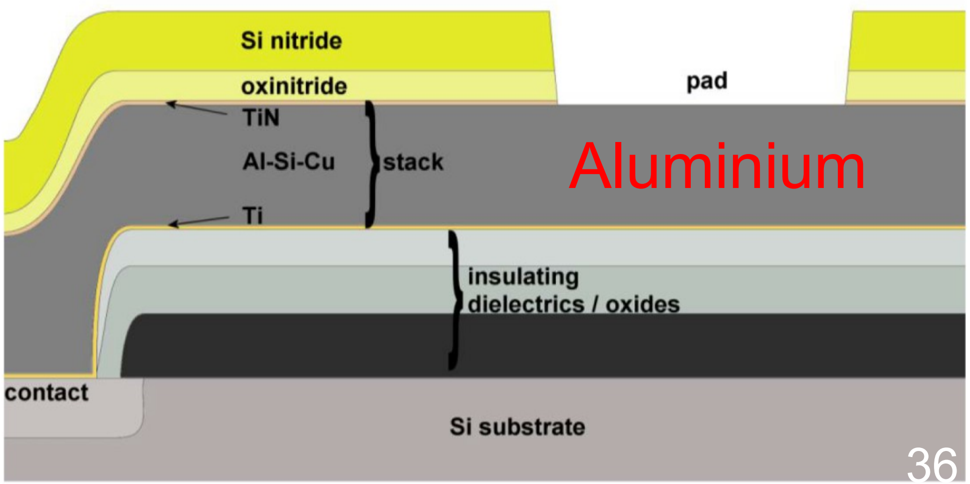
CMOS biochip

2+1 major components in a CMOS biochip



Hassibi, SiNano 2012

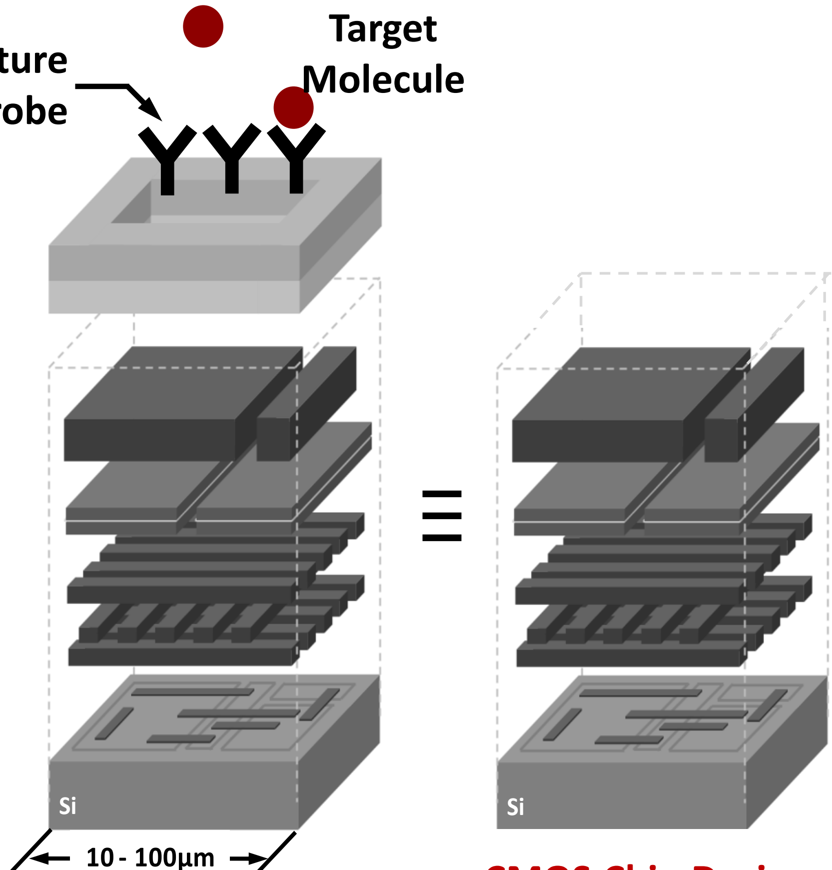
- oxide
- corrosion (Cl^-)
- biocompatibility?



Graham et al., Sensors p.4943, 2011

CMOS biochip

2+1 major components in a CMOS biochip



CMOS Chip Design
(Analog/Mixed-Mode IC Design)

\+

Post-CMOS Processing
(clean room)

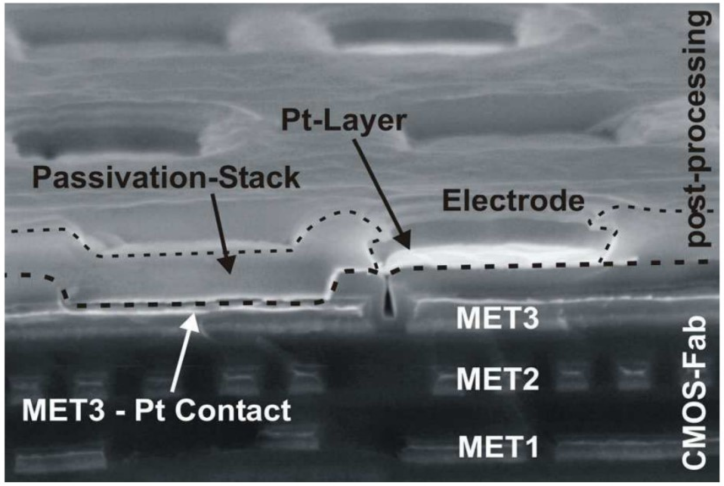
\+

Bio-functionalization
(Surface Chemistry/ Spotting Procedures)

Avoided if:
- Voltage meas.
- Impedance meas

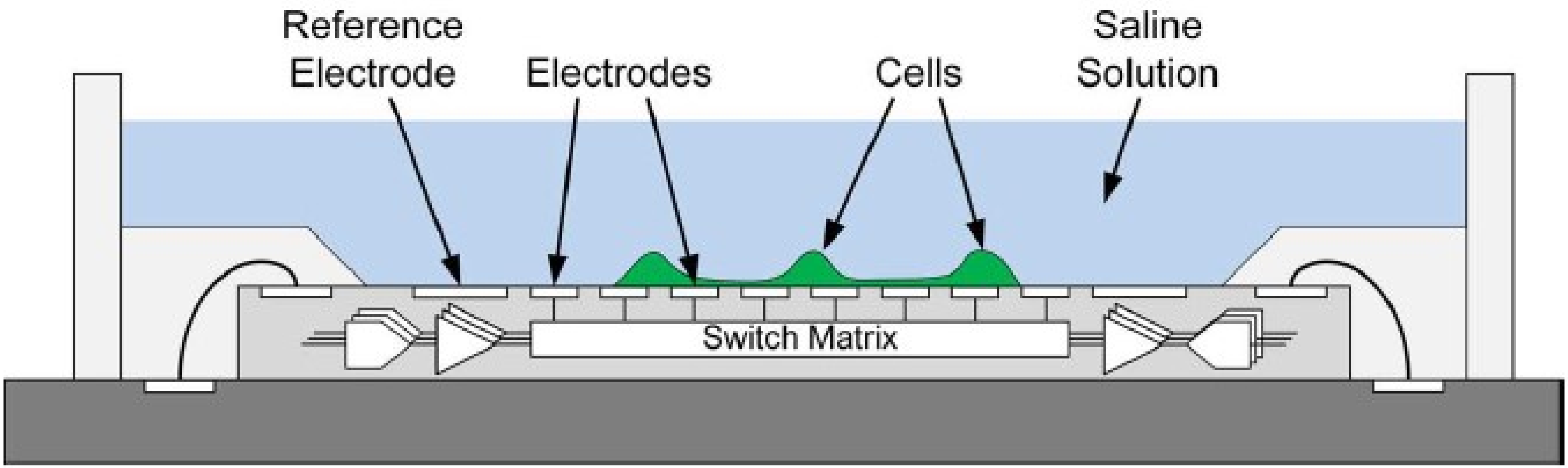
Hassibi, SiNano 2012

U. Frey, MEMS 2007



High-density MicroElectrode Array (MEA)

J. Dragas, V. Viswam, A. Shadmani, Y. Chen, R. Bounik, A. Stettler, M. Radivojevic, S. Geissler, M. E. J. Obien, J. Müller, and A. Hierlemann, “In Vitro Multi-Functional Microelectrode Array Featuring 59760 Electrodes, 2048 Electrophysiology Channels, Stimulation, Impedance Measurement, and Neurotransmitter Detection Channels,” *IEEE J. Solid-State Circuits*, vol. 52, no. 6, pp. 1576–1590, 2017



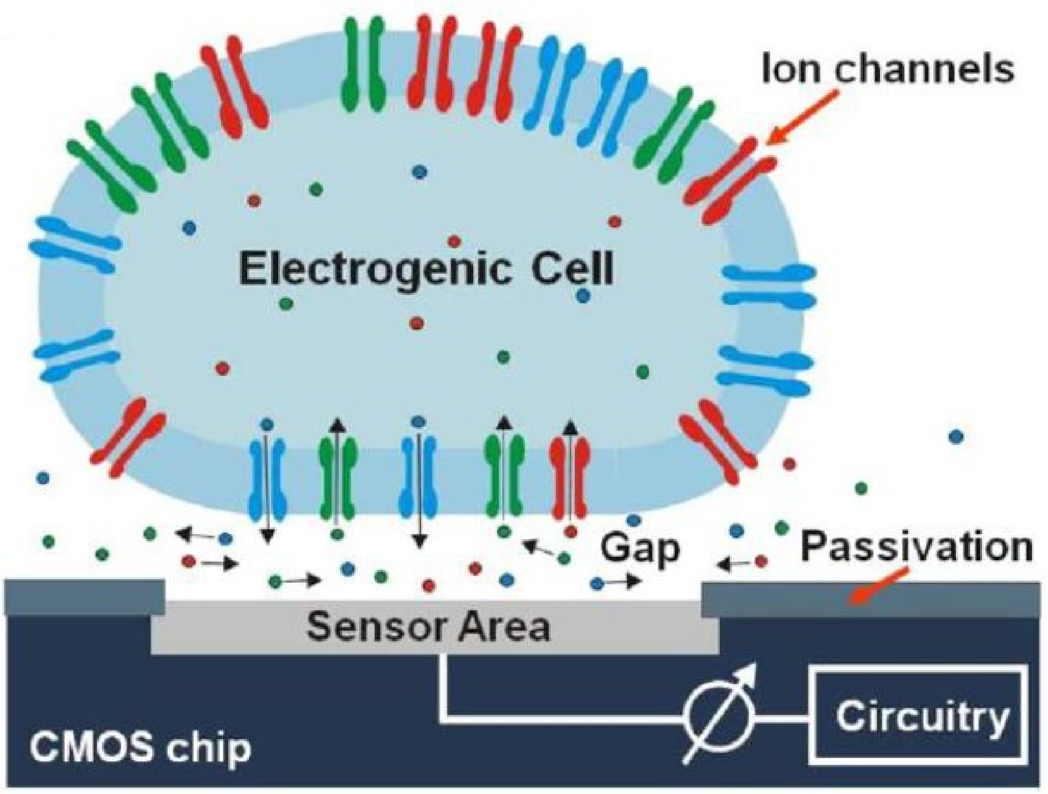
CMOS chip as active substrate for neural stimulation and recording

X. Yuan, A. Hierlemann, and U. Frey, “Extracellular Recording of Entire Neural Networks Using a Dual-Mode Microelectrode Array With 19,584 Electrodes and High SNR,” *IEEE J. Solid-State Circuits*, pp. 1–10, 2021

D. Tsai, D. Sawyer, A. Bradd, R. Yuste, and K. L. Shepard, “A very large-scale microelectrode array for cellular-resolution electrophysiology,” *Nat. Commun.*, vol. 8, no. 1, 2017

C. Laborde, F. Pittino, H. A. Verhoeven, S. G. Lemay, L. Selmi, M. A. Jongsma, and F. P. Widdershoven, “Real-time imaging of microparticles and living cells with CMOS nanocapacitor arrays.,” *Nat. Nanotechnol.*, vol. 10, no. 9, pp. 791–5, 2015.

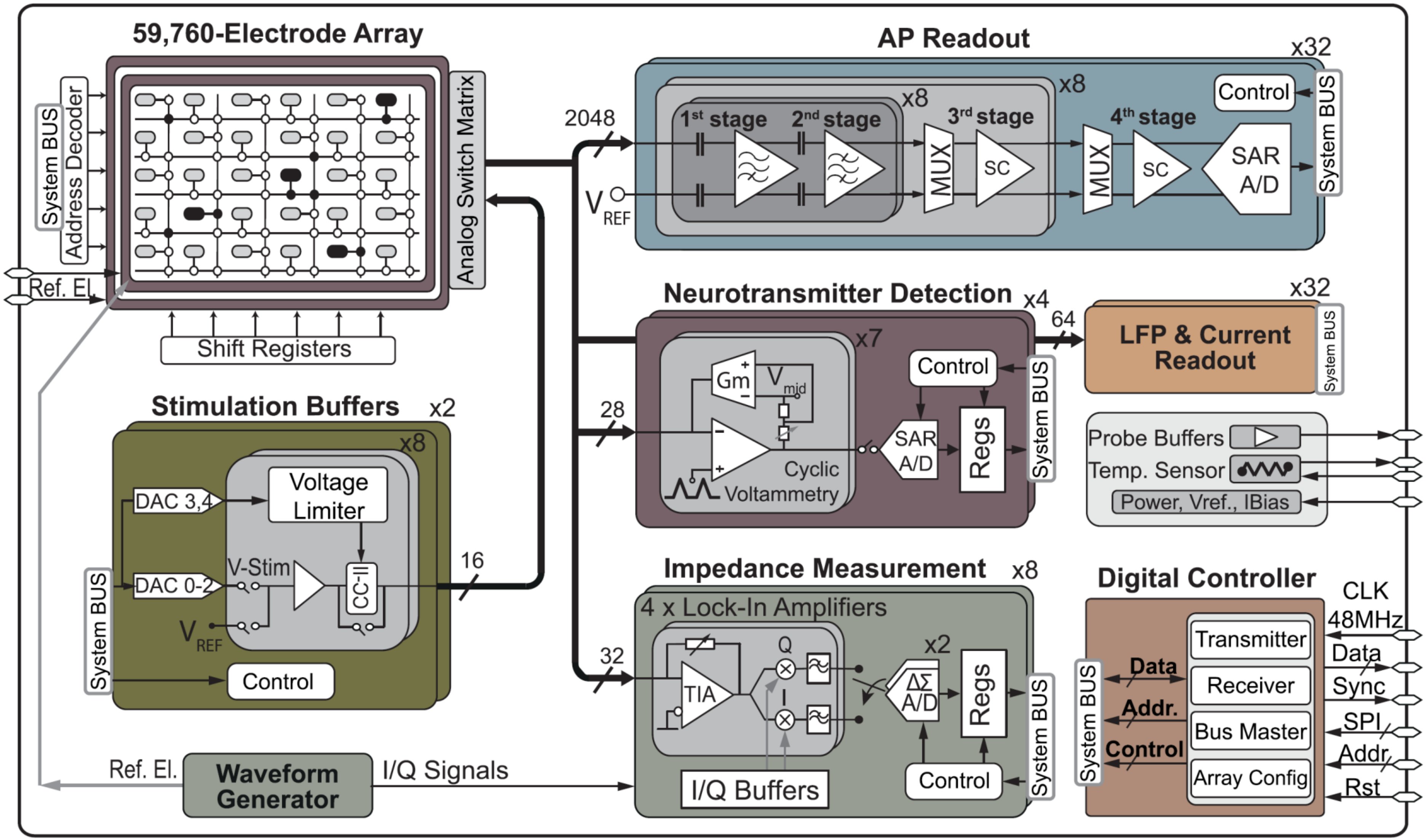
High-density MicroElectrode Array



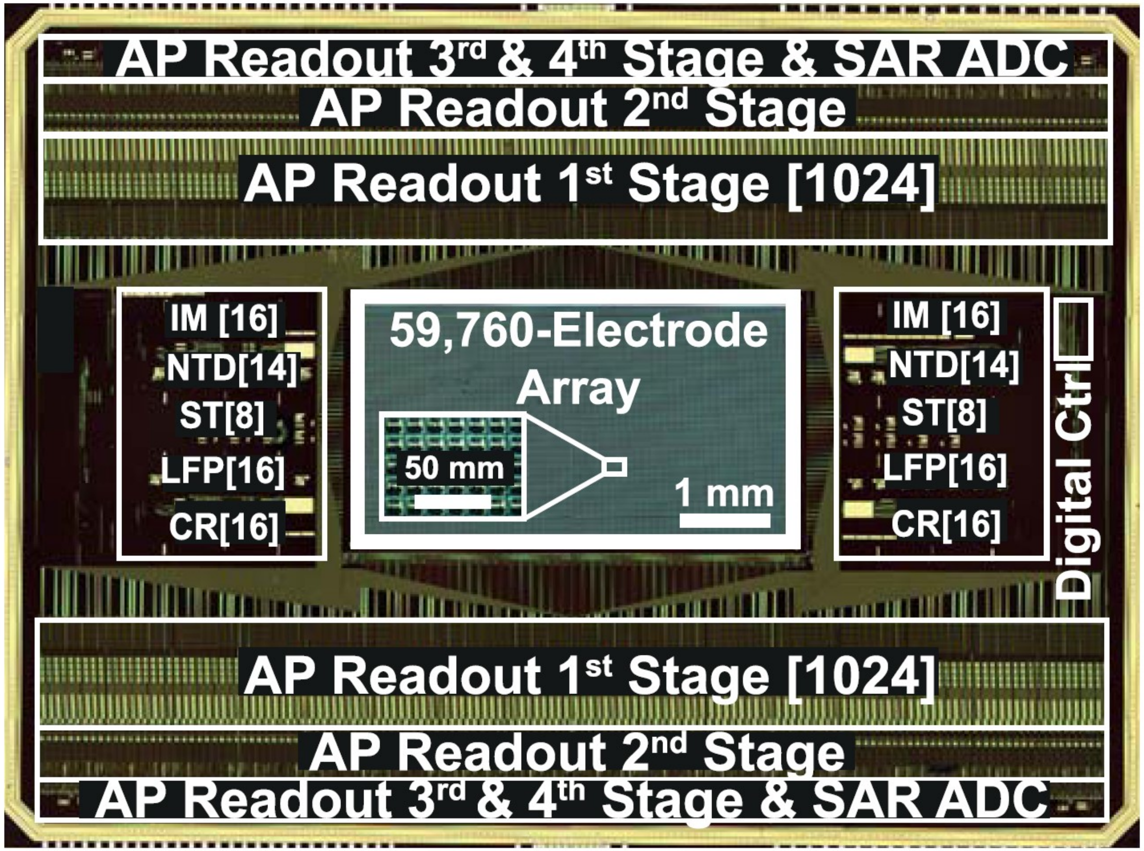
- Electrical stimulation
- Action potential recording
- Neurotransmitter detection (fast scan voltammetry)
- Impedance Spetroscopy (cells mapping)

M. Ballini, et al. *IEEE J. Solid-State Circuits*, vol. 49, no. 11, pp. 2705–2719, 2014.

High-density MicroElectrode Array

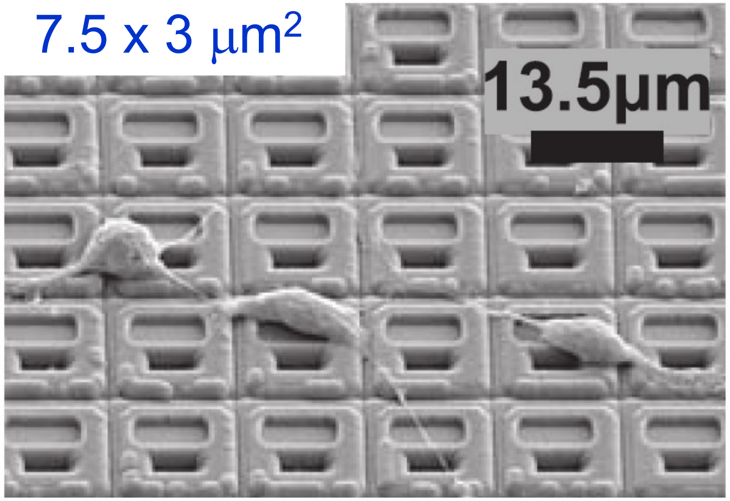


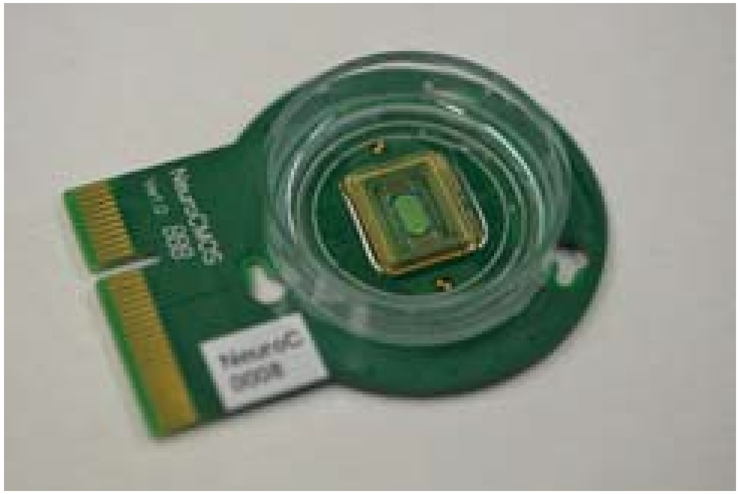
High-density MicroElectrode Array



180nm CMOS technology + post processing

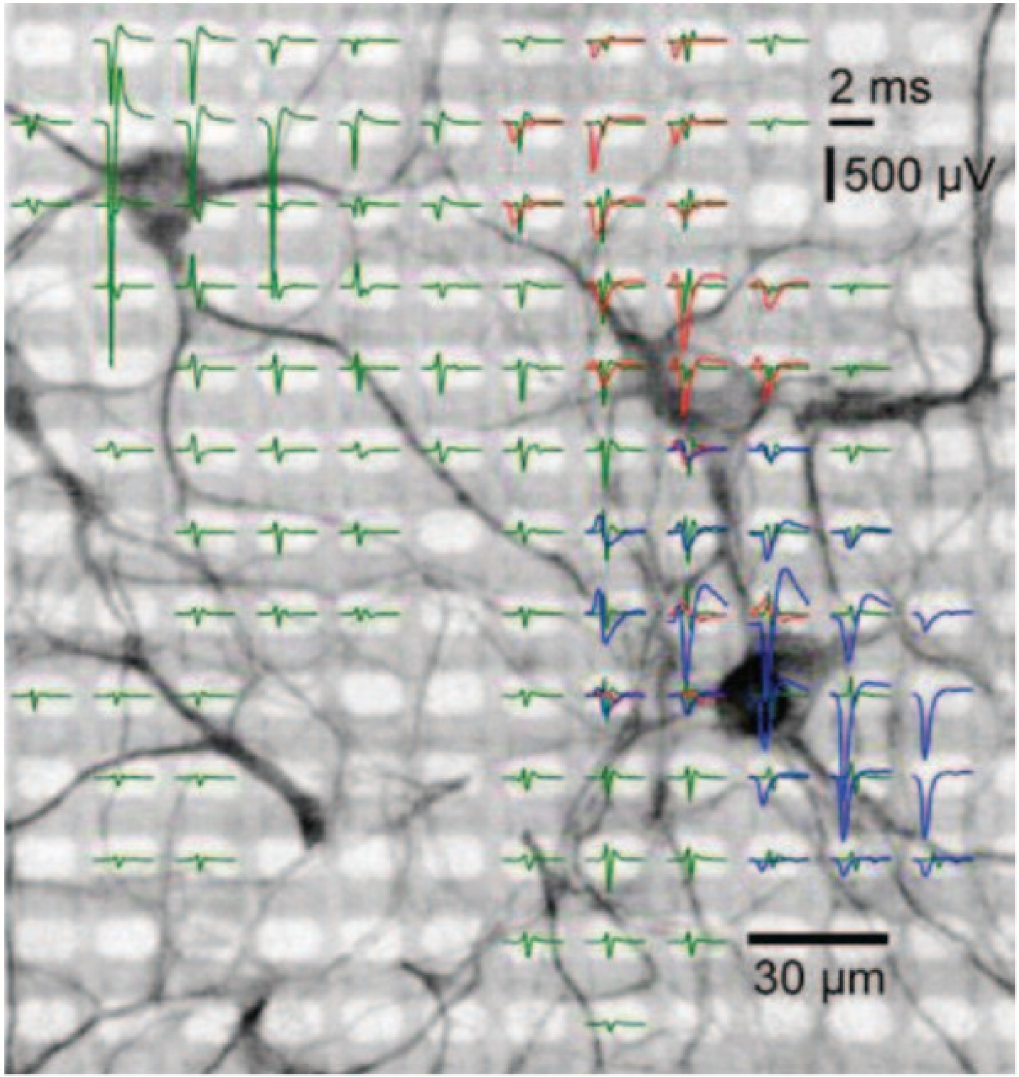
$7.5 \times 3\ \mu m^2$

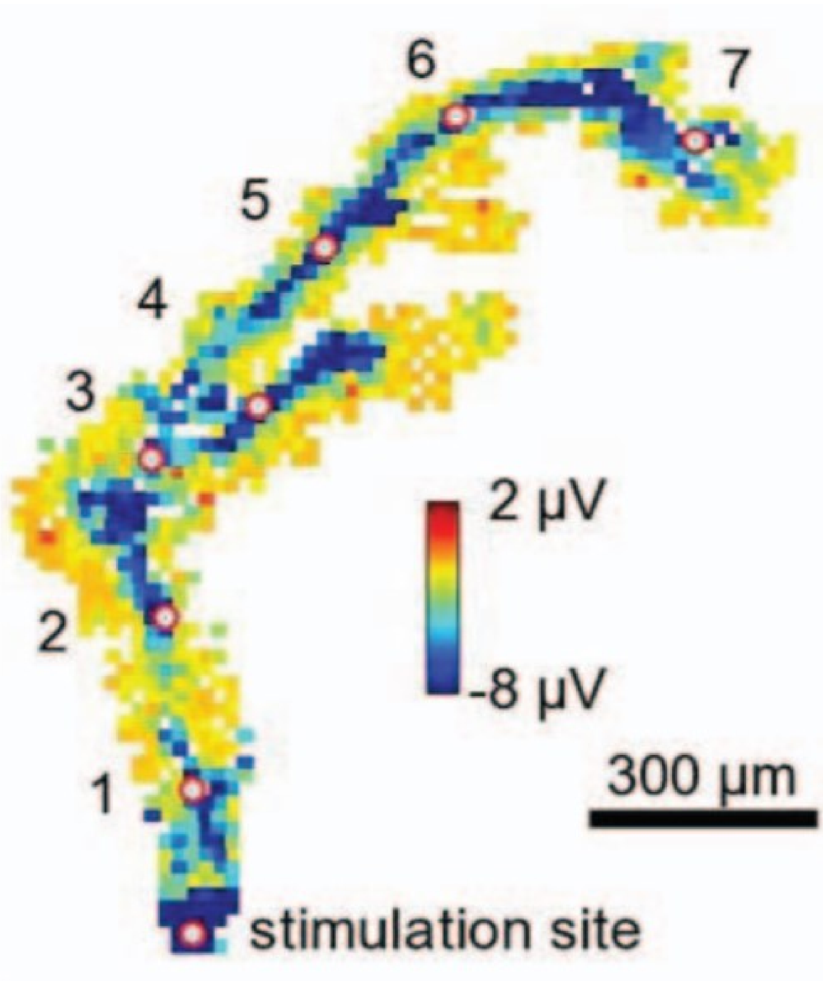




Chip: 12 x 8.9 mm^2; sensing area: 2.43 x 4.48 mm^2; power dissipation: 86mW

High-density MicroElectrode Array





A. Hierlemann, *Tech. Dig. - Int. Electron Devices Meet. IEDM*, 2016

Conclusions

- High-sensitivity instruments on a chip are feasible
- They enable new applications thanks to:
  - Improved performance (noise and/or power and/or speed)
  - Multichannel capability
  - Compactness
  - Access to microelectronic technology for on-chip sensors (some post-processing could be required)
- Co-design of sensor and electronics: no general-purpose chip!